

Nano Active Stabilization System - Instrumentation

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The goal is to show that each element in the system has been properly chosen based on certain requirements.

In order to determine the maximum noise of each instrumentation, a dynamic error budgeting is performed in Section ??.

The required instrumentation are then selected based on obtained noise specifications and other requirements summarized in Section 2.

The received instrumentation are characterized in Section 3.

- Say the the real time controller is a Speedgoat machine, as it is the standard real time controller used at the ESRF

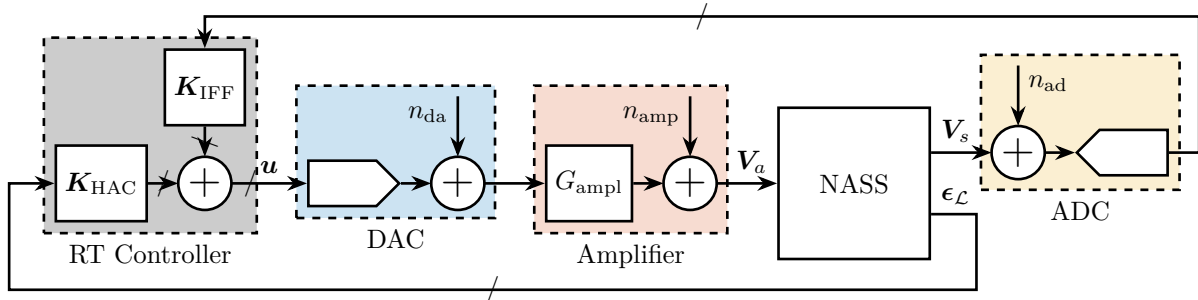


Figure 1: Block diagram of the NASS with considered instrumentation

1 Dynamic Error Budgeting

Goal:

- Write specifications regarding the maximum noise of instrumentation (ADC, DAC and voltage amplifier) such that it induces acceptable vibrations levels

Procedure:

- Get closed-loop transfer functions from disturbance sources (noise of ADC, DAC and amplifier noise) to positioning error This is done using the multi-body model, with 2DoF APA model (having voltage input and outputs)
- Focus is made on the vertical direction, as it is the direction with the most stringent requirements. If horizontal directions are considered, requirements are just less stringent than for the vertical direction.
- Deduce the maximum acceptable ASD of the noise sources

As the voltage amplifier gain will impact how the DAC noise will be amplified, some assumption are made:

- we want to apply -20 to 150V to the stacks
- Typical ADC are +/-10V
- Assumption of voltage amplifier with gain 20

1.1 Closed-Loop Sensitivity to Instrumentation Disturbances

The following noise sources are considered (Figure 1):

- n_{da} : output voltage noise of the DAC
- n_{amp} : output voltage noise of the voltage amplifier
- n_{ad} : voltage noise of the ADC measuring the force sensor stacks

Encoder noise, only used to estimate R_z is found to have little impact on the vertical sample error and is therefore omitted from this analysis for clarity.

The transfer function from these three noise sources (for one strut) to the vertical error of the sample are estimated from the multi-body model, including the APA300ML and the designed flexible joints

(Figure 1.1).

The lateral error was also considered, but the specifications are less stringent than vertical error and the sensitivity to disturbances is smaller.

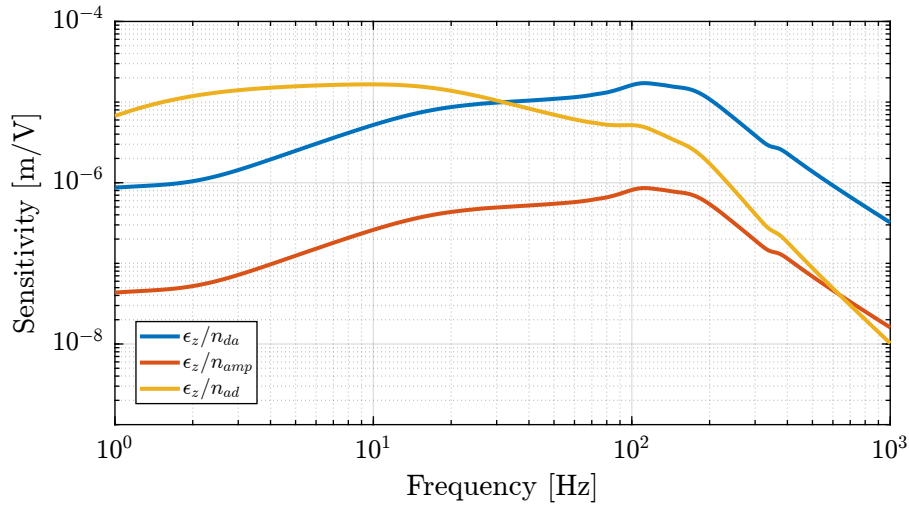


Figure 1.1: Transfer function from noise sources to vertical motion errors

1.2 Estimation of maximum instrumentation noise

From previous analysis, we know how the noise of the instrumentation will affect the vertical error of the sample. Now, we want to determine specifications for each instrumentation such that the effect on the vertical error of the sample is within specifications.

Most stringent requirement:

- vertical vibrations less than the smallest expected beam size of 100nm
- This corresponds to a maximum allowed vibration of 15nm RMS

Assumption on the noise:

- uncorrelated, which is reasonable. This means that the PSD of the different noise sources adds up.

Use of system symmetry to simplify the analysis:

- the effect of all the struts on the vertical errors are identical (verify from the extracted sensitivity curves). Therefore only one strut can be considered for this analysis, and the total effect of the six struts is just six times the effect of one strut (in terms of power, but in terms of RMS value it's only $\sqrt{6}=2.5$)

In order to have specifications for the noise of the instrumentation, assumptions:

- flat noise, which is quite typical

The noise specification is computed such that if all the instrumentation have this maximum noise, the specification in terms of vertical error is still respected. This is a pessimistic choice, but it gives a rough idea of the specifications.

Obtained maximum noise are:

- DAC maximum output noise ASD $14 \mu V / \sqrt{Hz}$.
- Voltage amplifier maximum output voltage noise ASD $280 \mu V / \sqrt{Hz}$
- ADC maximum measurement noise ASD $11 \mu V / \sqrt{Hz}$.

In terms of RMS noise,

- DAC: ± 1 mV RMS
- Voltage amplifier: ± 20 mV RMS
- ADC: ± 0.8 mV RMS

Table 1.1: Obtained specification in terms of noise

	ADC	DAC	Amplifier
Maximum ASD	$11 \mu V / \sqrt{Hz}$	$14 \mu V / \sqrt{Hz}$	$280 \mu V / \sqrt{Hz}$
RMS Noise	$0.8 mV$ RMS	$1 mV$ RMS	$20 mV$ RMS

If the Amplitude Spectral Density of the noise of the ADC, DAC and voltage amplifiers are all below the specified maximum noises, then the induced vertical error will be below 15nmRMS.

2 Choice of Instrumentation

In previous section: noise characteristics. In this section, other characteristics (range, bandwidth, etc...)

ADC, DAC, Voltage amplifier, Encoder

Model of each instrument (transfer function + noise source).

In this section, also tell which instrumentation has been bought, and different options.

block diagram of the model of the amplifier

2.1 Piezoelectric Voltage Amplifier

There are several characteristics of the piezoelectric voltage amplifiers that should be considered. To be able to use the full stroke of the piezoelectric actuator, the voltage output should be between -20 and 150V. It should accept an analog input voltage, preferably between -10 and 10V.

Small signal Bandwidth and Output Impedance There are two bandwidth that should be considered for a piezoelectric voltage amplifier: large signal bandwidth and small signal bandwidth. Large signal bandwidth are linked to the output current capacities of the amplifier and will be discussed next.

Small signal bandwidth of the voltage amplifier is very important for feedback applications as it can limit the bandwidth of the complete feedback system.

A simplified electrical model of a voltage amplifier connected to a piezoelectric stack is shown in Figure 2.1. This model is only valid for small signals, but it well models the small signal bandwidth limitation **fleming14'desig'model'contr'nanop'system**. R_o corresponds to the output impedance of the amplifier. With the piezoelectric load that corresponds to a capacitance C_p , it forms a first order low pass filter (2.1).

$$\frac{V_a}{V_i}(s) = \frac{1}{1 + \frac{s}{\omega_0}}, \quad \omega_0 = \frac{1}{R_o C_p} \quad (2.1)$$

Therefore, the small signal bandwidth is load dependent. As the capacitance load of the two piezoelectric stacks correspond to a capacitance $C_p = 8.8 \mu F$. If a small signal bandwidth of $f_0 = \frac{\omega_0}{2\pi} = 5 kHz$ is wanted, it corresponds to a maximum output impedance of $R_0 = 3.6 \Omega$.

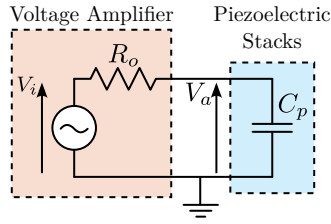


Figure 2.1: Electrical model of a voltage amplifier with output impedance R_0 connected to a piezoelectric stack with capacitance C_p

Large signal Bandwidth Large signal bandwidth are linked to the maximum output capabilities of the amplifiers in terms of amplitude as a function of frequency **spengen16'high'voltag'amplif**.

As the primary objective of the NASS is to stabilize the position and not to perform scans, this specification is not as important as the small signal bandwidth.

However, let's take into account scanning capabilities. In the worst case: constant velocity scan (i.e. triangular reference signal) with a repetition rate of $f_r = 100$ Hz and using full voltage capabilities of the piezoelectric actuator $V_{pp} = 170$ V.

There are two things to consider:

- Slew rate that should be above $2 \cdot V_{pp} \cdot f_r = 34$ V/ms This specification is easily achieved
- Current output capabilities: as the capacitance impedance decreases the the inverse of the frequency, it can reach very low values at high frequency In order to reach high voltage at high frequency, the required current that the voltage amplifier needs to provide may reach very large values. $I_{\max} = 2 \cdot V_{pp} \cdot f \cdot C_p = 0.3$ A

Output voltage noise As discussed in Section 1, the output noise of the voltage amplifier should be smaller than 20 mV RMS.

As explained in **spengen20'high'voltag'amplif**, the load capacitance of the piezoelectric stack filters the output noise of the amplifier (low pass filter of Figure 2.1). Therefore, when comparing noise of different voltage amplifiers, it should be noted what capacitance of the load is considered (i.e. the low signal bandwidth considered).

Here, the output noise should be smaller than 20mVRMS for a load of 8.8uF.

Choice of voltage amplifier The specifications as well as the amplifier characteristics as shown in the datasheet are summarized in Table 2.1.

The most important characteristics are the (small signal) bandwidth ≈ 5 [kHz] and the output voltage noise (≈ 20 [mV RMS]).

- Issue for the selection: manufacturers are not specifying the output noise as a function of frequency (i.e. the ASD of the noise), but only the RMS value (i.e. the integrated value over all frequency). It does not take into account the frequency dependency of the noise, that is very important to

perform error budgets. Also, the load the estimate the bandwidth and noise is often not mentioned (or no load for the bandwidth, and high capacitive load for the noise).

- Explain why the PD200 was selected:
 - fulfill the specification
 - clear documentation, especially about noise and bandwidth (Figure 2.2)

Table 2.1: Characteristics of the PD200 compared with the specifications

Specification	PD200	WMA-200	LA75B	E-505
Input Voltage Range: $\pm 10 V$	$\pm 10 V$	$\pm 8.75 V$	$-1/7.5 V$	
Output Voltage Range: $-20/150 V$	$-50/150 V$	$\pm 175 V$	$-20/150 V$	$-30/130$
Gain	20	20	20	10
Output Current $> 50 mA$	$900 mA$	$150 mA$	$360 mA$	$215 mA$
Slew Rate $> 34 V/ms$	$150 V/\mu s$	$80 V/\mu s$	n/a	n/a
Output noise (10uF load) $< 20 mV RMS$	$0.7 mV RMS (10 \mu F \text{ load})$	$0.05 mV (10 \mu F \text{ load})$	$3.4 mV$	$0.6 mV$
Small Signal Bandwidth (10 μF load): $> 5 kHz$	$6.4 kHz (10 \mu F \text{ load})$	$300 Hz^1$	$30 kHz (unloaded)$	n/a
Output Impedance: $< 3.6 \Omega$	n/a	$50 \Omega^1$	n/a	n/a

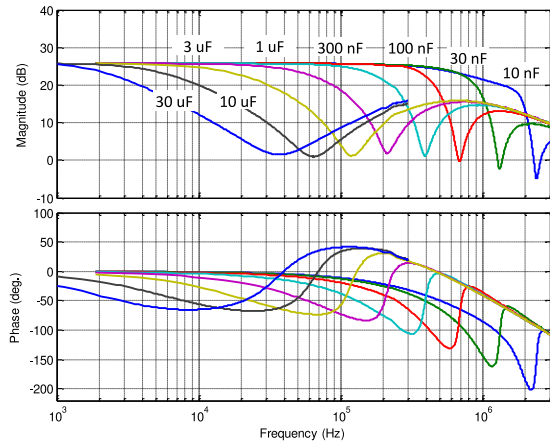
2.2 ADC and DAC

Synchronicity and Jitter For control systems, it is very important that the inputs and outputs are sampled synchronously with the controller and with low jitter. **abramovitch22'pract'method'real'world'contr'system, abramovitch23'tutor'real'time'comput'issues'contr'system.**

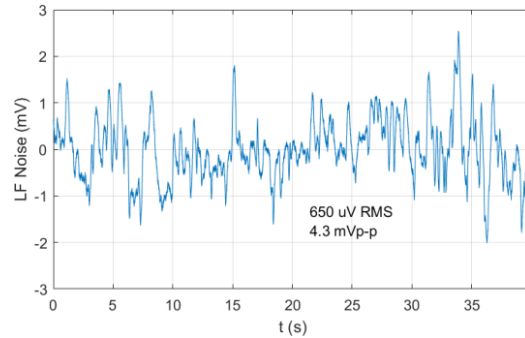
Therefore, the ADC and DAC:

- Needs to be well interfaced with the Speedgoat
- Sampling frequency of 10kHz
- Synchronous with the Speedgoat

¹The manufacturer proposed to remove the 50Ω output resistor to improve to small signal bandwidth above $10 kHz$



(a) sub caption a



(b) sub caption b

Figure 2.2: Caption with reference to sub figure (a)

Sampling Frequency, Bandwidth and delays Several requirements that may appear the same but are different:

- Sampling frequency: defines the interval between two sampled points, also determines the Nyquist frequency
- Bandwidth: defines the maximum frequency of a measured signal (typically specified as the -3dB point), usually limited by implemented anti-aliasing filters
- Delay/latency: delay between the analog signal at the input of the ADC to the digital information transferred to the control system

Sigma-Delta ADC can have extremely good noise characteristics, high bandwidth and sampling frequency but very poor latency. Typically, the latency can reach 20 times the sampling period **schmidt20' desig'high'perf**

Therefore, Sigma-Delta ADC are very well used for signal acquisition, but has limited use for real-time control where latency is critical. Therefore, for real time control applications, SAR-ADC (Successive approximation ADCs) is still the mostly applied type because of its single sample latency.

ADC Noise From the dynamical error budget in Section 1 Measurement noise ASD should be bellow $11\mu\text{V}/\sqrt{\text{Hz}}$, 0.8mV RMS

Linearity is not a concerned as it is not used for positioning but only for active damping So the accuracy of the measurement is not a concern

ADC are affected by various noise sources One of them is quantization noise, and is linked to the fact that input/output values can only take a finite number of values. Let's first find the number of bits such that the quantization noise is fulfilling the requirements.

Let's first suppose that the ADC is ideal and the only noise comes from the quantization error. Interestingly, the noise amplitude is uniformly distributed.

Let's note:

- $q = \frac{\Delta V}{2^n}$ the quantization in [V], which is the corresponding value in [V] of the least significant bit
- ΔV is the full range of the ADC in [V]
- n is the number of ADC's bits
- f_s is the sample frequency in [Hz]

The quantization noise can take a value between $\pm q/2$, and the probability density function is constant in this range (i.e., it's a uniform distribution). Since the integral of the probability density function is equal to one, its value will be $1/q$ for $-q/2 < e < q/2$ (Fig. 2.3).

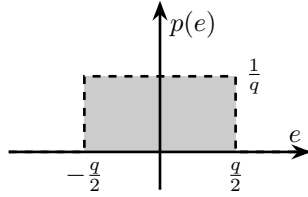


Figure 2.3: Probability density function $p(e)$ of the ADC error e

Now, we can calculate the time average power of the quantization noise as

$$P_q = \int_{-q/2}^{q/2} e^2 p(e) de = \frac{q^2}{12} \quad (2.2)$$

The other important parameter of a noise source is the power spectral density (PSD), which indicates how the noise power spreads in different frequency bands. To find the power spectral density, we need to calculate the Fourier transform of the autocorrelation function of the noise.

Assuming that the noise samples are not correlated with one another, we can approximate the autocorrelation function with a delta function in the time domain. Since the Fourier transform of a delta function is equal to one, the power spectral density will be frequency independent (i.e. white noise). Therefore, the quantization noise is white noise with total power equal to $P_q = \frac{q^2}{12}$.

Thus, the two-sided PSD (from $-\frac{f_s}{2}$ to $\frac{f_s}{2}$), we should divide the noise power P_q by f_s :

$$\int_{-f_s/2}^{f_s/2} \Gamma(f) df = f_s \Gamma = \frac{q^2}{12} \quad (2.3)$$

Finally, the Power Spectral Density of the quantization noise of an ADC is equal to:

$$\begin{aligned} \Gamma &= \frac{q^2}{12f_s} \\ &= \frac{\left(\frac{\Delta V}{2^n}\right)^2}{12f_s} \quad \text{in} \quad \left[\frac{V^2}{Hz} \right] \end{aligned} \quad (2.4)$$

The minimum number of bits so that the quantization noise is above some define values can be computed using:

$$n_{\min} = \log_2 \left(\frac{\Delta V}{\sqrt{12 F_s \Phi_{\max}}} \right) \quad (2.5)$$

With a sampling frequency $F_s = 10 \text{ kHz}$, a full range of $\Delta V = 20 \text{ V}$ and a maximum allowed ASD $\Phi_{\max} = 11 \mu\text{V}/\sqrt{\text{Hz}}$, the minimum number of bits is $n_{\min} = 12.4$, which is easily satisfied.

DAC Output voltage noise Similarly, the DAC output voltage noise ASD should be below $14 \mu\text{V}/\sqrt{\text{Hz}}$, 1mV RMS. This corresponds to a 13bits +/-10V DAC.

Choice of the ADC and DAC Board Based on the above analysis, the choice of ADC and DAC is quite simple.

Integrated in Speedgoat for best synchronicity. Chosen model: IO131:

- 16 analog inputs, based on the AD7609
 - 16 bits, +/- 10V
 - Maximum sampling rate of 200kSPS
 - Simultaneous sampling
 - Differential inputs: can use shielded twisted pairs for high noise immunity
- 8 analog outputs, based on the AD5754R
 - 16 bits, +/- 10V
 - Conversion time 10us
 - Simultaneous update

Noise is not specified, but as it has 16 bits resolution, it should be well below the requirements. It will be experimentally measured in Section 3.

2.3 Relative Displacement Sensors

Specifications:

- used for relative positioning
- Small enough to be integrated in each strut
- vertical errors of 15nmRMS = 6nmRMS for each strut = 6nmRMS sensor noise

- Stroke j 100um

There are many different sensors that can fulfil the requirements **fleming13'review'nanom'resol'posit'sensor:**

- Encoders
- Capacitive Sensors
- Eddy current sensors

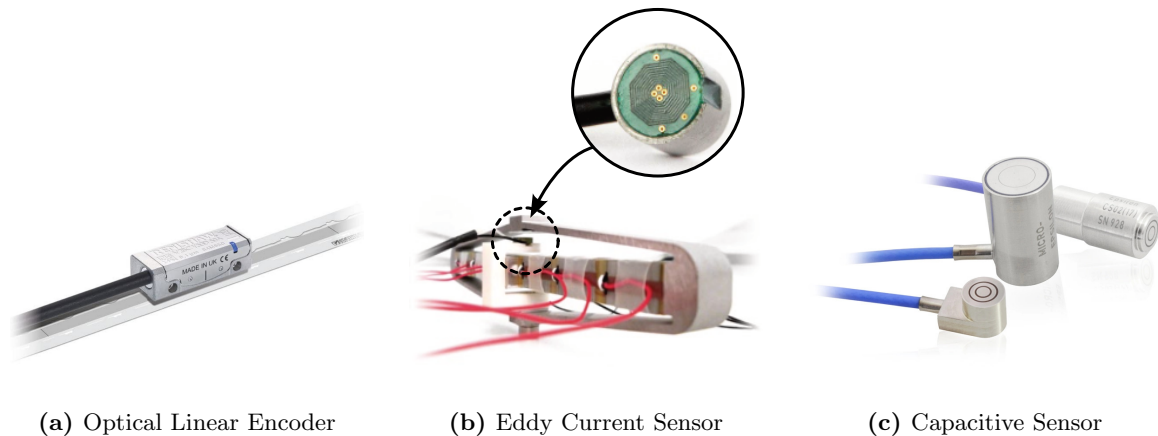


Figure 2.4: Measurement of strut flexible modes

The implementation:

- slight advantage to capacitive or eddy current sensors as they can measure in line with the APA (Figure 2.5b)
- for the encoder, the measurement has to be “offset” from the strut “action line”, and therefore relative rotations between the two ends of the APA induces measurement errors (Figure 2.5a).

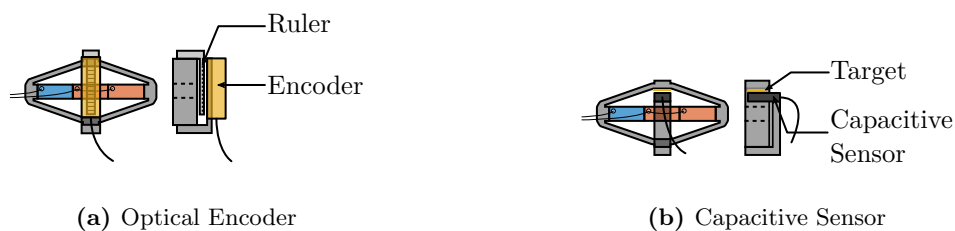


Figure 2.5: Caption with reference to sub figure

One major issue is the fact that the sensor signals have to pass through an electrical slip-ring (because of the continuous spindle rotation). Some measurements were performed on the slip-ring integrated in the micro-station, and the cross-talk between different slip-ring channels were found to be quite high. It was preferred to use a sensor that transmit the measured displacement digitally, such that it is much less sensitive to noise and cross-talk. For that reason, an optical encoder with digital output was preferred (i.e. the interpolation is performed directly in the head).

The specifications are summarized in Table 2.2.

Table 2.2: Characteristics of the Vionic compared with the specifications

Specification	Vionic	LION CPL190	Cedrat ECP500
Bandwidth	500 kHz	10kHz	20kHz
> 5 kHz			
Noise	1.6 nm rms	4 nm rms	15 nm rms
< 6 nm RMS			
Range Ruler length		250 um	500um
> 100 μm			
In line mea- sure- ment		×	
Digital Out- put	×		

3 Characterization of Instrumentation

All the instrumentation was then procured and tested individually to verify whether it fulfils the specifications or not.

Code couleur:

Yellow	ADC
Rouge	PD200
Vert	Femto
blue	DAC

Make sure that at some point I talk about twisted pairs etc.. Maybe use the nice schematic?

3.1 Analog to Digital Converters

Internally uses the AD7609 ADC from Analog Devices. 200kSPS, 16 bits, +/-10V

Measured Noise The ADC noise of the IO131 was simply measured by short-circuiting its input with a 50 Ohm resistor. Results are shown in Figure 3.1. The ADC noise is a white noise with an amplitude spectral density of $5.6 \mu V/\sqrt{Hz}$.

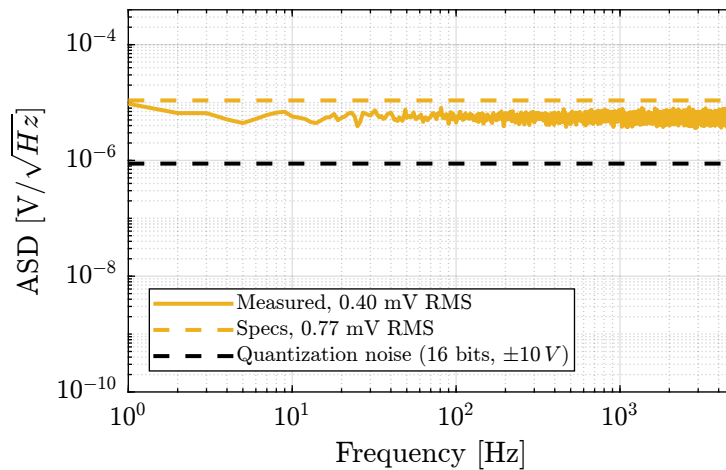


Figure 3.1: Measured ADC noise (IO318)

If required, it is possible to apply some oversampling to lower the obtained noise **lab13'improv'adc**. To have additional w bits of resolution, the oversampling frequency f_{os} should be:

$$f_{os} = 4^w \cdot f_s \tag{3.1}$$

As the ADC can work at 200kSPS, and we only need 10kSPS, we can have an oversampling factor of 16 and have two more bits of resolution (i.e. reducing the noise by a factor 4). This works because the noise can be approximated by a white noise and the amplitude is larger than 1 LSB (0.3 mV) **hauser91'princ'overs'conver**.

Reading of piezoelectric force sensor There are few other things to consider when measuring the voltage generated by a piezoelectric stack.

The setup is shown in Figure 3.2 where two stacks are used as actuator (in parallel) and one stack is used as sensor. The voltage amplifier used has a gain of 20 [V/V].

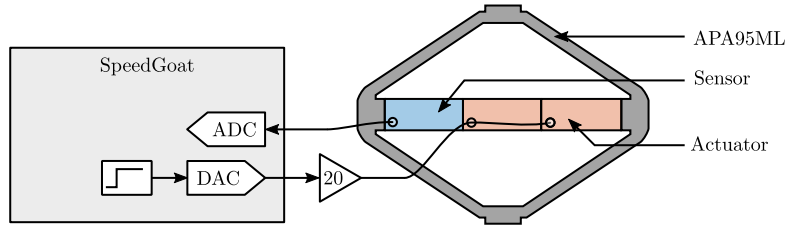


Figure 3.2: Schematic of the setup

The excitation signal (steps) and measured voltage across the sensor stack are shown in Figure 3.3. The measured voltage shows an exponential decay which indicates that the charge across the capacitor formed by the stack is discharging into a resistor. This corresponds to an RC circuit with a time constant $\tau = R_i C_p$. Therefore, first order high filter, with corner frequency $1/\tau$.

The exponential curves are fitted and a value of $\tau = 6.5 s$ and an offset voltage of $2.26 V$ are found.

With the capacitance being $C_p = 4.4 \mu F$, the internal impedance of the Speedgoat ADC can be computed as follows $R_i = \frac{\tau}{C_p} = 1.5 M\Omega$.

It is close to the specified value of $1 M\Omega$ found in the datasheet

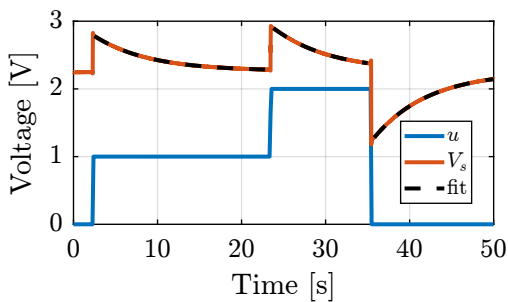


Figure 3.3: Translation Stage

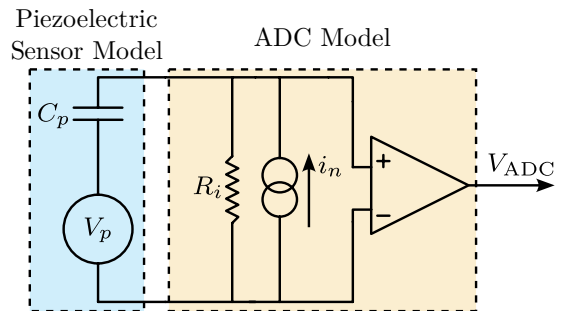


Figure 3.4: Tilt Stage

As shown in Figure 3.3, the voltage across the Piezoelectric sensor stack shows a constant voltage offset. This can be explained by looking at the electrical model shown in Figure 3.4 (taken from **reza06'piezoel'trans'vibrat'contr'dampin**).

The differential amplifier in the Speedgoat has some input bias current i_n that induces a voltage offset V_{off} across its own internal resistance R_i . Note that the impedance of the piezoelectric stack is much

larger than that at DC.

Therefore, the input bias current i_n is estimated from $i_n = V_{\text{off}}/R_i = 1.5 \mu\text{A}$.

In order to reduce the input voltage offset and to increase the corner frequency of the high pass filter, a resistor is added in parallel to the force sensor.

- Reduction of input voltage offset:

$$V_{\text{off}} = \frac{R_a R_{in}}{R_a + R_{in}} i_n$$

- Increase the high pass corner frequency f_c

$$C_p \frac{R_{in} R_a}{R_{in} + R_a} = \tau_c = \frac{1}{f_c}$$

$$R_a = \frac{R_i}{f_c C_p R_i - 1}$$

The resistor is chosen such that the high pass corner frequency is equal to 3Hz. This corresponds to a resistor of $R_p = 80 \text{ k}\Omega$.

With this parallel resistance value, the voltage offset would be $V_{\text{off}} = 0.11 \text{ V}$, which is much more acceptable.

To validate this, a resistor $R_p \approx 82 \text{ k}\Omega$ is then added in parallel with the force sensor as shown in Figure 3.6. After the resistor is added, the same steps response is performed. And indeed, we obtain a much smaller offset voltage ($V_{\text{off}} = 0.15 \text{ V}$) and a much faster time constant ($\tau = 0.45 \text{ s}$). This validates the model of the ADC and the effectiveness of the added resistor.

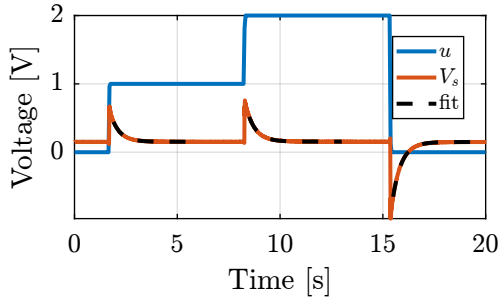


Figure 3.5: Translation Stage

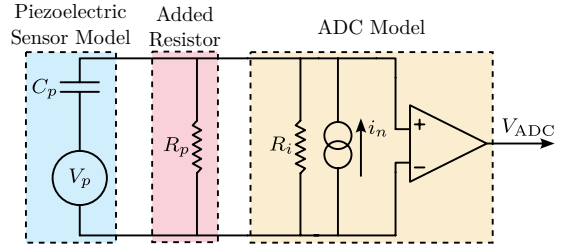


Figure 3.6: Tilt Stage

3.2 Instrumentation Amplifier

Because the ADC noise may be too large to measure noise of other instruments (anything below $5.6 \mu\text{V}/\sqrt{\text{Hz}}$ cannot be distinguish from the noise of the ADC itself), a low noise instrumentation amplifier can be used.

Different instrumentation amplifiers were used:

- EG&G 5113, 4nV/sqrt(Hz), gain up to 100000 (100dB)
- Femto DLPVA-101-B-S 2nV/sqrt(Hz), gain from 20 to 80dB
- Koheron AMP200, 2.4nV/sqrt(Hz), gain up to 100

Here, the Femto amplifier is used.

But first, the input noise of the amplifier is characterized.

- Footnote: for variable gain amplifiers, it is more convenient to refer to the input noise rather than the output noise.

Its input is short circuited, and the output voltage is measured by the ADC. The maximum amplifier gain of 80dB (i.e. 10000) is used.

The measured voltage is then divided by 10000 to obtain the equivalent noise at the input of the voltage amplifier. In that case, the noise of the ADC is negligible, thanks to the high gain used.

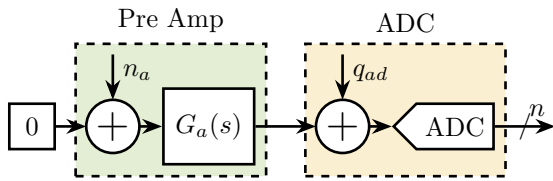


Figure 3.7: Translation Stage

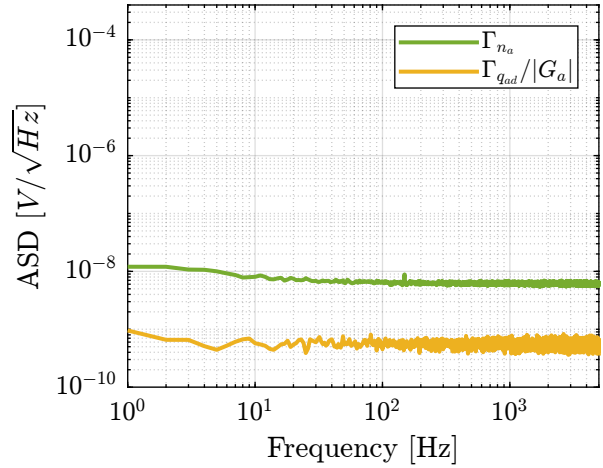


Figure 3.8: Tilt Stage

3.3 Digital to Analog Converters

Noise Measurement In order not to have any quantization noise and only measure the output voltage noise of the DAC, we “ask” the DAC to output a zero voltage.

The measurement setup is schematically represented in Figure 3.9. The gain of the pre-amplifier is adjusted such that the measured amplified noise is much larger than the quantization noise of the ADC.

The Amplitude Spectral Density $\Gamma_n(\omega)$ of the measured signal is computed. The Amplitude Spectral Density of the DAC output voltage noise n_{da} can be computed taking into account the gain of the pre-amplifier:

$$\Gamma_{n_{da}}(\omega) = \frac{\Gamma_m(\omega)}{|G_a(\omega)|} \quad (3.2)$$

And it is verified that the Amplitude Spectral Density of n_{da} is much larger than the one of n_a :

$$\Gamma_{n_{da}} \gg \Gamma_{n_a} \quad (3.3)$$

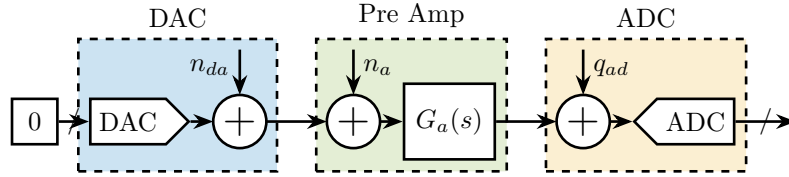


Figure 3.9: Figure caption

The obtained Amplitude Spectral Density of the DAC's output voltage is shown in Figure 3.10a. It is almost white noise with an ASD of 0.6uV/sqrt(Hz). There is a little bit of 50Hz, and some low frequency noise (thermal noise?) which are not foreseen to be an issue as it will be inside the bandwidth.

DAC is directly wired to the ADC. The transfer function from DAC to ADC is computed. It corresponds to 1 sample delay (Figure 3.10b).

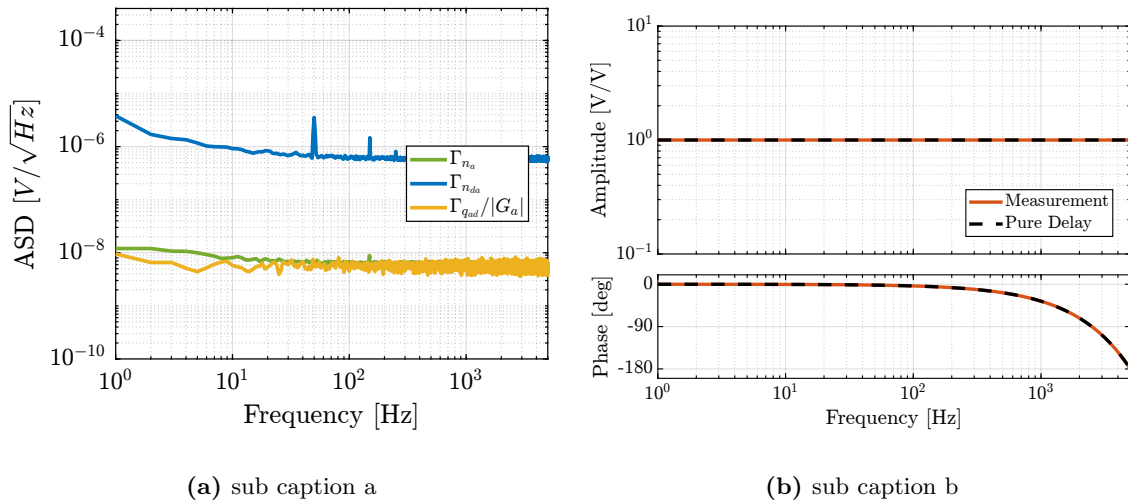


Figure 3.10: Measure transfer function from DAC to ADC - It fits a pure “1-sample” delay (??)

3.4 Piezoelectric Voltage Amplifier

Output Voltage Noise The measurement setup is shown in Figure 3.11. The input of the PD200 amplifier is shunted with a 50 Ohm resistor such that there is no voltage input expected the PD200 input voltage noise. The gain of the pre-amplifier is increased in order to measure a signal much larger than the quantization noise of the ADC.

Two piezoelectric stacks of the APA95ML are connected to the PD200 output to have appropriate load.

The measured low frequency (>20Hz) **output** noise of one of the PD200 amplifiers is shown in Figure 3.12. It is very similar to the one specified in the datasheet in Figure ??.

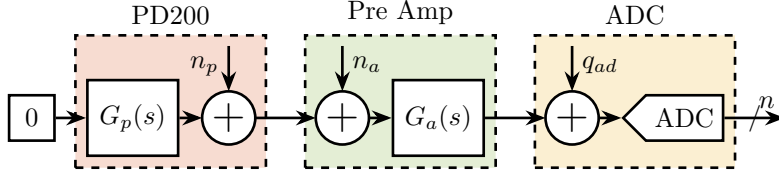


Figure 3.11: Sources of noise in the experimental setup

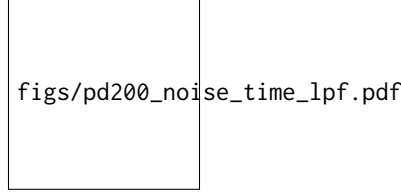


Figure 3.12: Measured low frequency noise of the PD200 from 0.01Hz to 20Hz

The obtained RMS and peak to peak values of the measured **output** noise are shown in Table ?? and found to be very similar to the specified ones.

	RMS [μV]	Peak to Peak [mV]
Specification [$10 \mu F$]	714.0	4.3
PD200 1	565.1	3.7
PD200 2	767.6	3.5
PD200 3	479.9	3.0
PD200 4	615.7	3.5
PD200 5	651.0	2.4
PD200 6	473.2	2.7
PD200 7	423.1	2.3

The Amplitude Spectral Density $\Gamma_n(\omega)$ of the measured signal by the ADC is computed. The Amplitude Spectral Density of the input voltage noise of the PD200 amplifier n_p is then computed taking into account the gain of the pre-amplifier and the gain of the PD200 amplifier:

$$\Gamma_{n_p}(\omega) = \frac{\Gamma_n(\omega)}{|G_p(j\omega)G_a(j\omega)|} \quad (3.4)$$

And we verify that we are indeed measuring the noise of the PD200 and not the noise of the pre-amplifier by checking that:

$$\Gamma_{n_p}(\omega)|G_p(j\omega)| \ll \Gamma_{n_a} \quad (3.5)$$

The Amplitude Spectral Density of the measured **input** noise is computed and shown in Figure ??.

It is verified that the contribution of the PD200 noise is much larger than the contribution of the pre-amplifier noise of the quantization noise.

The Amplitude Spectral Density of the input noise of the PD200 amplifiers present sharp peaks. It is not clear yet what causes such peaks and if these peaks have high influence on the total RMS noise of the amplifiers.

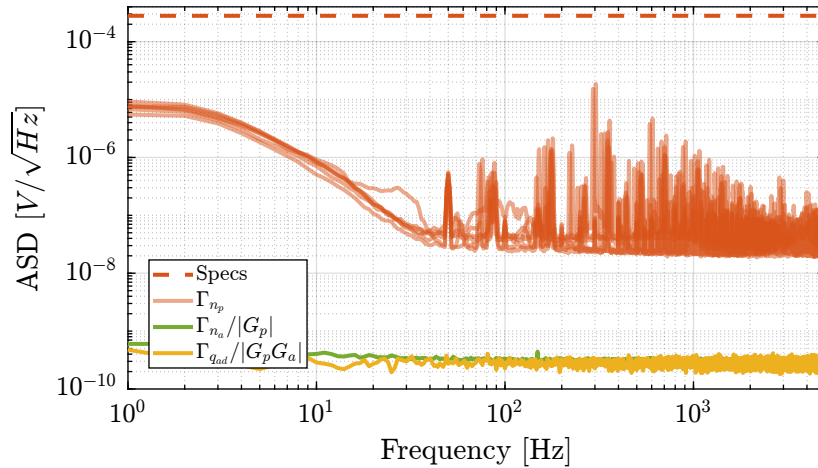


Figure 3.13: Measured output voltage noise of the PD200 amplifiers

Small Signal Bandwidth Here the small signal dynamics of all the PD200 amplifiers are identified.

A (logarithmic) sweep sine excitation voltage is generated by the Speedgoat DAC with an amplitude of 0.1V and a frequency going from 1Hz up to 5kHz.

The output voltage of the PD200 amplifier is measured thanks to the monitor voltage of the PD200 amplifier. The input voltage of the PD200 amplifier (the generated voltage by the DAC) is measured with another ADC of the Speedgoat. This way, the time delay related to the ADC will not be apparent in the results.

The obtained transfer functions from V_{in} to V_{out} are shown in Figure 3.14.

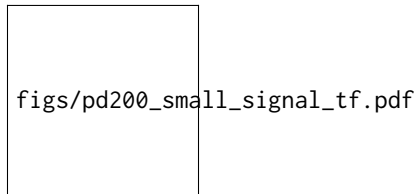


Figure 3.14: Identified dynamics from input voltage to output voltage

We can see the very well matching between all the 7 amplifiers. The amplitude is constant over a wide frequency band and the phase drop is limited to less than 1 degree up to 500Hz.

The identified dynamics in Figure 3.14 can very well be modeled this dynamics with a first order low pass filter (even a constant could work fine).

Output Impedance The goal of this experimental setup is to estimate the output impedance R_{out} of the PD200 voltage amplifiers. A DAC with a constant output voltage (here 0.1V) is connected to the input of the PD200 amplifier.

Then, the output voltage of the PD200 amplifier is measured in two conditions:

- V when the output is not connected to any load

- V_p when a load $R_{\text{load}} = 10 \Omega$ is connected at the output of the amplifier

The load and the output impedance form a voltage divider, and thus:

$$V' = \frac{R}{R + R_{\text{out}}} V$$

From the two values of voltage, the output impedance of the amplifier can be estimated:

$$R_{\text{out}} = R_{\text{load}} \frac{V - V_p}{V} \quad (3.6)$$

From this measurement, all the PD200 amplifiers are found to have an output impedance $R_{\text{out}} \approx 1 \Omega$.

With the capacitive load $C_p = 8.8 \mu F$, the output resistor of the amplifier forms a low pass filter with a corner frequency equal to $f_0 = \frac{1}{R_{\text{out}} C_p}$. We get a corner frequency around 10 kHz which is not far from the specified 7.4 kHz.

Table 3.1: Measured characteristics, Manual characteristics and specified ones

Characteristics	Measurement	Manual	Specification
Input Voltage Range	-	+/- 10 [V]	+/- 10 [V]
Output Voltage Range	-	-50/150 [V]	-20/150 [V]
Gain		20 [V/V]	-
Maximum RMS current		0.9 [A]	∓ 50 [mA]
Maximum Pulse current		10 [A]	-
Slew Rate		150 [V/us]	-
Noise (10uF load)		0.7 [mV RMS]	∓ 2 [mV rms]
Small Signal Bandwidth (10uF load)		7.4 [kHz]	∓ 5 [kHz]
Large Signal Bandwidth (150V, 10uF)		300 [Hz]	-

Conclusion

3.5 Linear Encoders

To measure the noise n of the encoder, one can rigidly fix the head and the ruler together such that no motion should be measured. Then, the measured signal y_m corresponds to the noise n .

The measurement bench is shown in Figures 3.15 and 3.16. Note that the bench is then covered with a “plastic bubble sheet” in order to keep disturbances as small as possible.

Then, and for all the 7 encoders, we record the measured motion during 100s with a sampling frequency of 20kHz.

3.6 External Metrology

[test-bench-attocube](#)

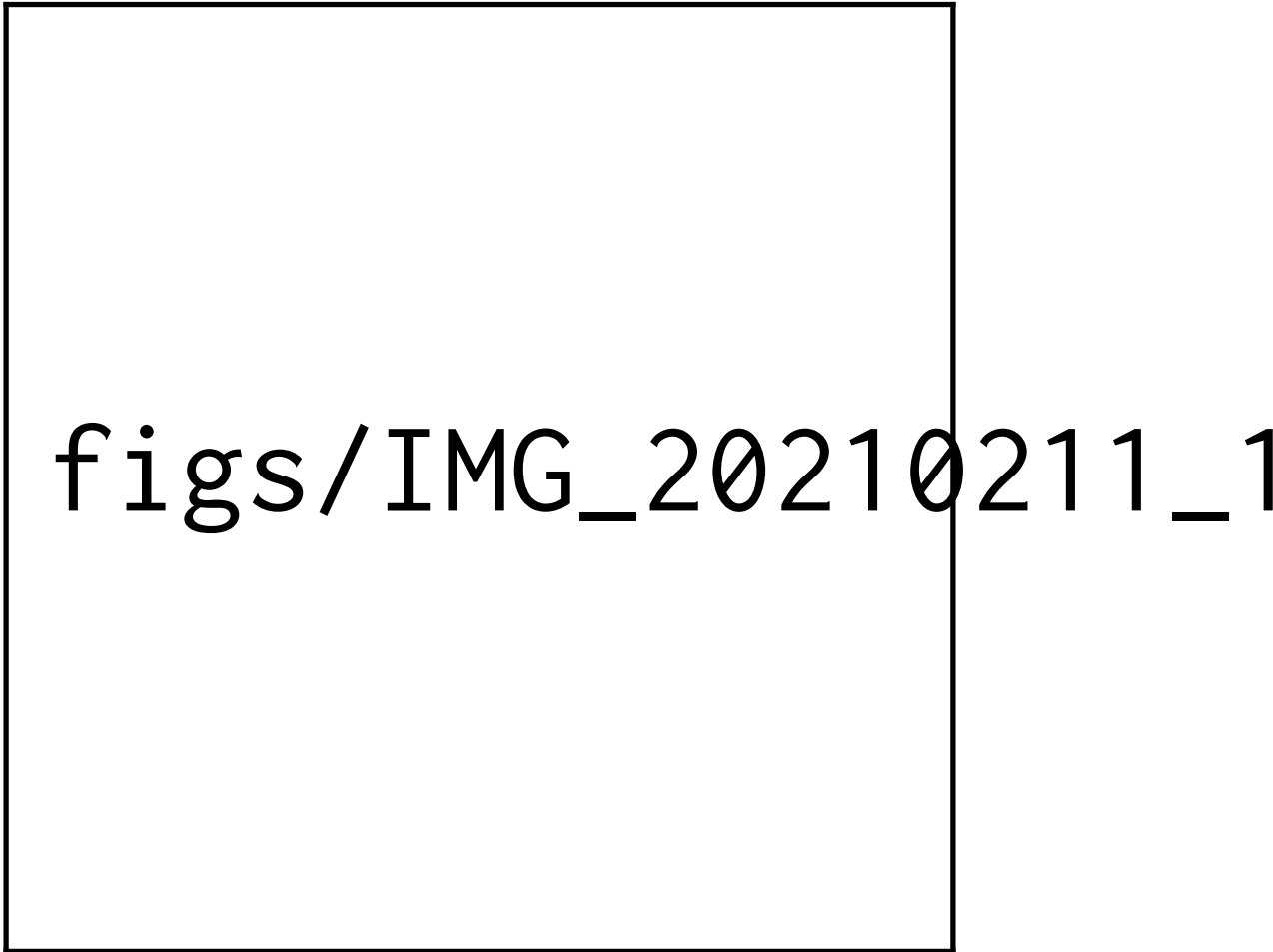



Figure 3.15: Top view picture of the measurement bench



figs/IMG_20210211_1

Figure 3.16: Side view picture of the measurement bench

Different options:

- Attocube: issue of non-linearity estimated from the encoders
- Smaract
- QuDIS

For the final tests, QuDIS were used.

3.7 Conclusion

From all the measured noises, compute the obtained PSD error in Y and Z (show PSD of individual + Sum + Cumulative?)

Conclusion