

# **Nano Active Stabilization System - Instrumentation**

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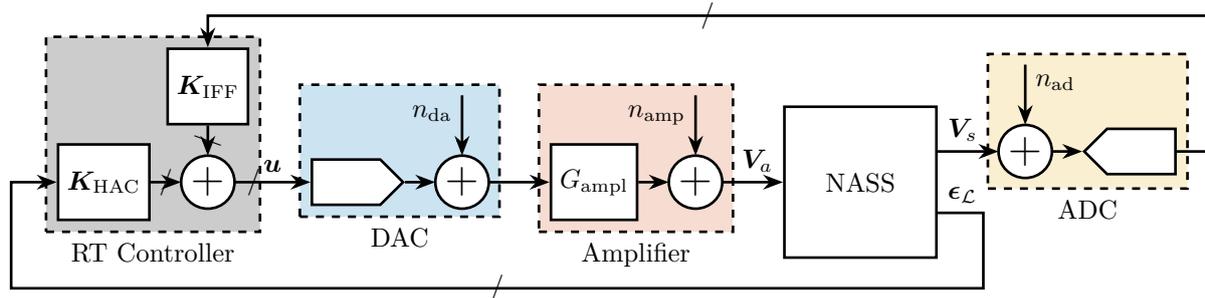
The goal is to show that each element in the system has been properly chosen based on certain requirements.

In order to determine the maximum noise of each instrumentation, a dynamic error budgeting is performed in Section ??.

The required instrumentation are then selected based on obtained noise specifications and other requirements summarized in Section 2.

The received instrumentation are characterized in Section 3.

- Say the the real time controller is a Speedgoat machine, as it is the standard real time controller used at the ESRF



**Figure 1:** Block diagram of the NASS with considered instrumentation

# 1 Dynamic Error Budgeting

## Goal:

- Obtain specifications regarding the maximum noise of instrumentation (ADC, DAC and voltage amplifier) such that it induces acceptable vibrations levels

## Procedure:

- Get closed-loop transfer functions from noise sources (noise of ADC, DAC and amplifier noise) to positioning error. This is done using the multi-body model, with 2DoF APA model (having voltage input and outputs).
- Focus is made on the vertical direction, as it is the direction with the most stringent requirements. If horizontal directions are considered, requirements are just less stringent than for the vertical direction.
- Deduce the maximum acceptable ASD of the noise sources.

As the voltage amplifier gain will impact how the DAC noise is amplified, some assumption are made:

- we want to apply -20 to 150V to the stacks
- Typical ADC are +/-10V
- Assumption of voltage amplifier with gain 20

## 1.1 Closed-Loop Sensitivity to Instrumentation Disturbances

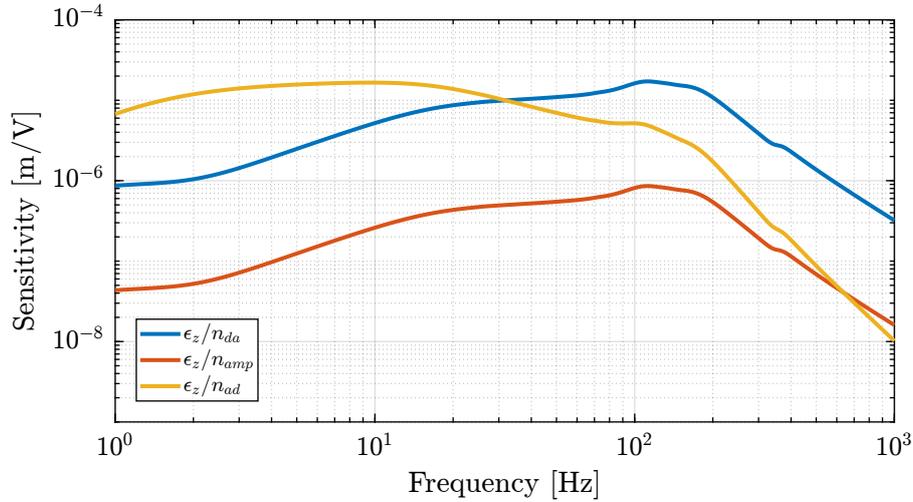
The following noise sources are considered (Figure 1):

- $n_{da}$ : output voltage noise of the DAC
- $n_{amp}$ : output voltage noise of the voltage amplifier
- $n_{ad}$ : voltage noise of the ADC measuring the force sensor stacks

Encoder noise, only used to estimate  $R_z$  is found to have little impact on the vertical sample error and is therefore omitted from this analysis for clarity.

The transfer function from these three noise sources (for one strut) to the vertical error of the sample are estimated from the multi-body model, including the APA300ML and the designed flexible joints (Figure 1.1).

The lateral error was also considered, but the specifications are less stringent than vertical error and the sensitivity to disturbances is smaller.



**Figure 1.1:** Transfer function from noise sources to vertical motion errors

## 1.2 Estimation of maximum instrumentation noise

From previous analysis, we know how the noise of the instrumentation will affect the vertical error of the sample as a function of frequency. Now, we want to determine specifications for each instrumentation such that the effect on the vertical error of the sample is within specifications.

Most stringent requirement:

- Vertical vibrations less than the smallest expected beam size of 100nm
- This corresponds to a maximum allowed vibration of 15nm RMS

Assumption on the noise:

- DAC, DAC and amplifier noise are uncorrelated, which is reasonable. Noise corresponding each strut are each uncorrelated. This means that the PSD of the different noise sources adds up.

Use of system symmetry to simplify the analysis:

- the effect of all the struts on the vertical errors are identical (verify from the extracted sensitivity curves). Therefore only one strut can be considered for this analysis, and the total effect of the six struts is just six times the effect of one strut (in terms of power, but in terms of RMS value it's only  $\sqrt{6}=2.5$ )

In order to have specifications in terms of noise spectral density of each instrumentation, a white noise is assumed, which is quite typical.

The noise specification is computed such that if all the instrumentation have this maximum noise, the specification in terms of vertical error is still respected. This is a pessimistic choice, but it gives a rough

idea of the specifications.

Obtained maximum noise are:

- DAC maximum output noise ASD  $14 \mu V / \sqrt{Hz}$ .
- Voltage amplifier maximum output voltage noise ASD  $280 \mu V / \sqrt{Hz}$
- ADC maximum measurement noise ASD  $11 \mu V / \sqrt{Hz}$ .

In terms of RMS noise,

- DAC:  $\pm 1$  mV RMS
- Voltage amplifier:  $\pm 20$  mV RMS
- ADC:  $\pm 0.8$  mV RMS

**Table 1.1:** Obtained specification in terms of noise

	ADC	DAC	Amplifier
Maximum ASD	$11 \mu V / \sqrt{Hz}$	$14 \mu V / \sqrt{Hz}$	$280 \mu V / \sqrt{Hz}$
RMS Noise	$0.8 mV$ RMS	$1 mV$ RMS	$20 mV$ RMS

If the Amplitude Spectral Density of the noise of the ADC, DAC and voltage amplifiers are all below the specified maximum noises, then the induced vertical error will be below 15nmRMS.

Such specification will guide the choice of instrumentation in Section 2.

## 2 Choice of Instrumentation

Based on:

- noise specifications extracted from Section 1
- other specifications (input/output range, bandwidth, etc. . .)

The most adequate ADC, DAC, Voltage amplifier, and relative positioning sensor are found. Different options that were considered are presented, and the choice of instrumentation is explained.

### 2.1 Piezoelectric Voltage Amplifier

There are several characteristics of the piezoelectric voltage amplifiers that should be considered. To be able to use the full stroke of the piezoelectric actuator, the voltage output should be between -20 and 150V. It should accept an analog input voltage, preferably between -10 and 10V, as it is quite typical for DAC.

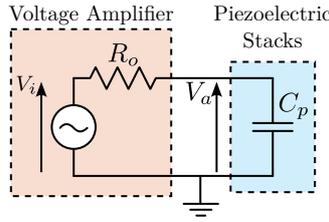
**Small signal Bandwidth and Output Impedance** There are two bandwidth that should be considered for a piezoelectric voltage amplifier: large signal bandwidth and small signal bandwidth. Large signal bandwidth are linked to the output current capacities of the amplifier and will be discussed next.

Small signal bandwidth of the voltage amplifier is very important for feedback applications as it can limit the bandwidth of the complete feedback system.

A simplified electrical model of a voltage amplifier connected to a piezoelectric stack is shown in Figure 2.1. This model is only valid for small signals, but it is useful to understand the small signal bandwidth limitation **fleming14'desig'model'contr'nano'p'system**.  $R_o$  corresponds to the output impedance of the amplifier. With the piezoelectric load that corresponds to a capacitance  $C_p$ , it forms a first order low pass filter (2.1).

$$\frac{V_a}{V_i}(s) = \frac{1}{1 + \frac{s}{\omega_0}}, \quad \omega_0 = \frac{1}{R_o C_p} \quad (2.1)$$

Therefore, the small signal bandwidth is load dependent (it decreases as the load capacitance increases). The capacitance load of the two piezoelectric stacks in the APA300ML correspond to a capacitance  $C_p = 8.8 \mu F$ . If a small signal bandwidth of  $f_0 = \frac{\omega_0}{2\pi} = 5 \text{ kHz}$  is wanted, the voltage amplifier output impedance should be smaller than  $R_0 = 3.6 \Omega$ .



**Figure 2.1:** Electrical model of a voltage amplifier with output impedance  $R_o$  connected to a piezoelectric stack with capacitance  $C_p$

**Large signal Bandwidth** Large signal bandwidth are linked to the maximum output capabilities of the amplifiers in terms of amplitude as a function of frequency **spengen16'high'voltag'amplif**.

As the primary objective of the NASS is to stabilize the position and not to perform scans, this specification is not as important as the small signal bandwidth.

However, let's take into account scanning capabilities, and consider the worst case scenario of a constant velocity scan (i.e. triangular reference signal) with a repetition rate of  $f_r = 100$  Hz and using full voltage capabilities of the piezoelectric actuator  $V_{pp} = 170$  V.

There are two things to consider:

- Slew rate that should be above  $2 \cdot V_{pp} \cdot f_r = 34$  V/ms This specification is easily achieved by commercial voltage amplifiers.
- Current output capabilities: as the capacitance impedance decreases the the inverse of the frequency, it can reach very low values at high frequency In order to reach high voltage at high frequency, the required current that the voltage amplifier needs to provide may reach very large values.  $I_{\max} = 2 \cdot V_{pp} \cdot f \cdot C_p = 0.3$  A

So ideally, a voltage amplifier capable of providing 0.3 A of current is wanted.

**Output voltage noise** As discussed in Section 1, the output noise of the voltage amplifier should be smaller than 20 mV RMS.

As explained in **spengen20'high'voltag'amplif**, the load capacitance of the piezoelectric stack filters the output noise of the amplifier (low pass filter of Figure 2.1). Therefore, when comparing noise indicated in the datasheet of different voltage amplifiers, it is important to check what is the considered capacitance of the load (i.e. the low signal bandwidth considered).

Here, the output noise should be smaller than 20mVRMS for a load of 8.8uF and a bandwidth larger than 5kHz.

**Choice of voltage amplifier** The specifications are summarized in Table 2.1. The most important characteristics being the (small signal) bandwidth  $\geq 5$  [kHz] and the output voltage noise ( $\leq 20$  [mV RMS]).

Several voltage amplifiers were considered, with datasheet information summarized in Table 2.1.

- Issue for the selection: manufacturers are not specifying the output noise as a function of frequency (i.e. the ASD of the noise), but only the RMS value (i.e. the integrated value over all frequency). It does not take into account the frequency dependency of the noise, that is very important to perform error budgets. Also, the load used to estimate the bandwidth and noise is often not mentioned. Most of the time, the bandwidth is indicated with very little load and the noise with high load. It renders the comparison between different models more complex.
- The chosen model is the PD200 from PiezoDrive.
  - It fulfill the specification
  - It has clear documentation, especially about noise and bandwidth

**Table 2.1:** Characteristics of the PD200 compared with the specifications

Specification	PD200 PiezoDrive	WMA-200 Falco	LA75B Cedrat	E-505 PI
Input Voltage Range: $\pm 10 V$	$\pm 10 V$	$\pm 8.75 V$	$-1/7.5 V$	
Output Voltage Range: $-20/150 V$	$-50/150 V$	$\pm 175 V$	$-20/150 V$	$-30/130$
Gain > 15	20	20	20	10
Output Current > 300 mA	900 mA	150 mA	360 mA	215 mA
Slew Rate > 34 V/ms	150 V/ $\mu s$	80 V/ $\mu s$	n/a	n/a
Output noise < 20 mV RMS (10 $\mu F$ load)	0.7 mV RMS (10 $\mu F$ load)	0.05 mV (10 $\mu F$ load)	3.4 mV	0.6 mV
Small Signal Bandwidth > 5 kHz (10 $\mu F$ load)	6.4 kHz (10 $\mu F$ load)	300 Hz <sup>1</sup>	30 kHz (unloaded)	n/a
Output Impedance: < 3.6 $\Omega$	n/a	50 $\Omega$ ??	n/a	n/a

## 2.2 ADC and DAC

Analog to digital converters and digital to analog converters are very important to convert signals from the RT controller that only uses digital numbers to the physical plant, which is of course affected by analog signals.

**Synchronicity and Jitter** For control systems, it is very important that the inputs and outputs are sampled synchronously with the controller and with low jitter **abramovitch22'pract'method'real'world'contr'system, abramovitch23'tutor'real'time'comput'issues'contr'system.**

Therefore, the ADC and DAC needs to be well interfaced with the Speedgoat, and triggered synchronously with the computation of the control signals. For that reason, it was decided to first look for ADC and DAC sold by Speedgoat (the RT controller used).

**Sampling Frequency, Bandwidth and delays** Several requirements may appear the same but are very different in nature:

<sup>1</sup>The manufacturer proposed to remove the 50  $\Omega$  output resistor to improve to small signal bandwidth above 10 kHz

- Sampling frequency: defines the interval between two sampled points, also determines the Nyquist frequency
- Bandwidth: defines the maximum frequency of a measured signal (typically specified as the -3dB point), usually limited by implemented anti-aliasing filters
- Delay/latency: delay between the analog signal at the input of the ADC to the digital information transferred to the control system

Sigma-Delta ADC can have extremely good noise characteristics, high bandwidth and sampling frequency but very poor latency. Typically, the latency can reach 20 times the sampling period **schmidt20'desig'high'perf**

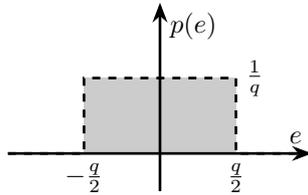
Therefore, Sigma-Delta ADC are very much used for signal acquisition applications, but has limited use for real-time control where latency is critical. Therefore, for real time control applications, SAR-ADC (Successive approximation ADCs) is still the mostly applied type because of its single sample latency.

**ADC Noise** From the dynamical error budget in Section 1 Measurement noise ASD should be bellow 11uV/sqrt(Hz), 0.8mV RMS

ADC are affected by various noise sources One of them is quantization noise, and is linked to the fact that input/output values can only take a finite number of values. Let's first find the number of bits such that the quantization noise is fulfilling the requirements.

Let's first suppose that the ADC is ideal and the only noise comes from the quantization error. Let's note  $q = \frac{\Delta V}{2^n}$  the quantization in [V], which is the corresponding value in [V] of the least significant bit.  $\Delta V$  is the full range of the ADC in [V],  $n$  is the number of ADC's bits and  $F_s$  is the sample frequency in [Hz].

The quantization noise can take a value between  $\pm q/2$ , and the probability density function is constant in this range (i.e., it's a uniform distribution). Since the integral of the probability density function  $p(e)$  is equal to one, its value is  $1/q$  for  $-q/2 < e < q/2$  as illustrated in Figure 2.2.



**Figure 2.2:** Probability density function  $p(e)$  of the ADC error  $e$

The variance (or time average power) of the quantization noise is (2.2).

$$P_q = \int_{-q/2}^{q/2} e^2 p(e) de = \frac{q^2}{12} \quad (2.2)$$

Now, the goal is to compute the power spectral density of the quantization noise, which is by definition the Fourier transform of the autocorrelation function of the quantization noise. Assuming that the noise samples are not correlated with one another, the autocorrelation function can be approximated with a delta function in the time domain. Since the Fourier transform of a delta function is equal to one,

the power spectral density will be frequency independent (i.e. white noise). Therefore, thanks to the Parseval's theorem, the quantization noise is a white noise with total power equal to  $P_q = \frac{q^2}{12}$ .

Thus, the two-sided PSD (from  $-\frac{F_s}{2}$  to  $\frac{F_s}{2}$ ), we should divide the noise power  $P_q$  by  $F_s$ :

$$P_q = \int_{-F_s/2}^{F_s/2} \Gamma(f) df = F_s \Gamma = \frac{q^2}{12} \quad (2.3)$$

Finally, the Power Spectral Density of the quantization noise of an ADC is equal to (2.4).

$$\Gamma_q = \frac{q^2}{12F_s} = \frac{\left(\frac{\Delta V}{2^n}\right)^2}{12F_s} \quad \text{in} \quad \left[ \frac{V^2}{\text{Hz}} \right] \quad (2.4)$$

From a defined noise amplitude spectral density  $\Phi_{\max}$ , the minimum number of bits so that the quantization noise is below  $\Phi_{\max}$  can be computed from (2.5).

$$n = \log_2 \left( \frac{\Delta V}{\sqrt{12F_s\Phi_{\max}}} \right) \quad (2.5)$$

With a sampling frequency  $F_s = 10 \text{ kHz}$ , a full range of  $\Delta V = 20 \text{ V}$  and a maximum allowed ASD  $\Phi_{\max} = 11 \mu\text{V}/\sqrt{\text{Hz}}$ , the minimum number of bits is  $n_{\min} = 12.4$ , which is easily satisfied by commercial ADCs.

**DAC Output voltage noise** Similarly to ADC, the DAC output voltage noise ASD should be below  $14 \mu\text{V}/\sqrt{\text{Hz}}$ , 1mV RMS. This corresponds to a 13bits +/-10V DAC, which is easily satisfied.

**Choice of the ADC and DAC Board** Based on the above analysis, the choice of ADC and DAC is quite straightforward.

Integrated in Speedgoat for best synchronicity. Chosen model: IO131:

- 16 analog inputs, based on the AD7609
  - 16 bits, +/- 10V
  - Maximum sampling rate of 200kSPS
  - Simultaneous sampling
  - Differential inputs: can use shielded twisted pairs for high noise immunity
- 8 analog outputs, based on the AD5754R
  - 16 bits, +/- 10V
  - Conversion time 10us

- Simultaneous update

Noise is not specified, but as it has 16 bits resolution, it should be well below the requirements. It will be experimentally measured in Section 3.

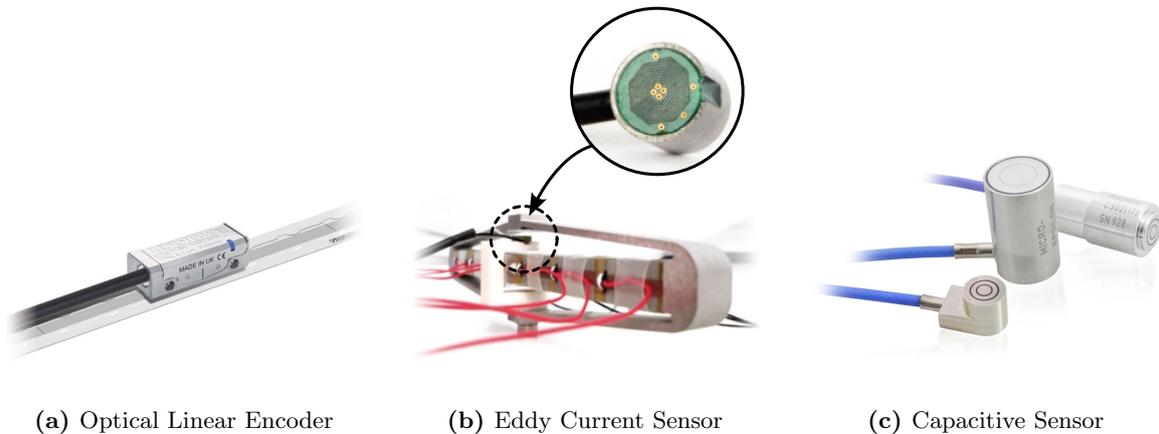
## 2.3 Relative Displacement Sensors

Specifications:

- used for relative positioning
- Small enough to be integrated in each strut
- vertical errors of 15nmRMS  $\Rightarrow$  6nmRMS for each strut  $\Rightarrow$  maximum 6nmRMS sensor noise
- Stroke  $\geq$  100um

There are many different sensors that can fulfil the requirements **fleming13'review'nanom'resol'posit'sensor:**

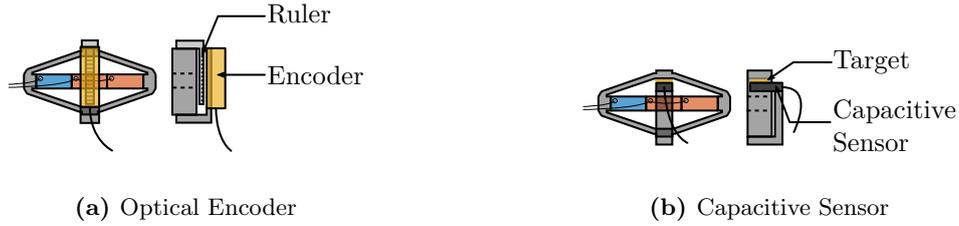
- Encoders
- Capacitive Sensors
- Eddy current sensors



**Figure 2.3:** Measurement of strut flexible modes

The implementation:

- slight advantage to capacitive or eddy current sensors as they can measure in line with the APA (Figure 2.4b)
- for the encoder, the measurement has to be “offset” from the strut “action line”, and therefore relative rotations between the two ends of the APA induces measurement errors (Figure 2.4a).



**Figure 2.4:** Caption with reference to sub figure

One major issue is the fact that the sensor signals have to pass through an electrical slip-ring (because of the continuous spindle rotation). Some measurements were performed on the slip-ring integrated in the micro-station, and the cross-talk between different slip-ring channels were found to be quite high. It was preferred to use a sensor that transmit the measured displacement digitally, such that it is much less sensitive to noise and cross-talk. For that reason, an optical encoder with digital output was preferred (i.e. the interpolation is performed directly in the head).

The specifications are summarized in Table 2.2.

**Table 2.2:** Characteristics of the Vionic compared with the specifications

Specification	Renishaw Vionic	LION CPL190	Cedrat ECP500
Technology	Digital Encoder	Capacitive	Eddy Current
Bandwidth > 5 kHz	> 500 kHz	10kHz	20kHz
Noise < 6 nm RMS	1.6 nm rms	4 nm rms	15 nm rms
Range > 100 $\mu\text{m}$	Ruler length	250 $\mu\text{m}$	500 $\mu\text{m}$
In line measurement		×	×
Digital Output	×		

## 3 Characterization of Instrumentation

All the instrumentation was then procured and tested individually to verify whether it fulfils the specifications or not.

### 3.1 Analog to Digital Converters

The ADC of the IO318 cards:

- have differential inputs
- internally uses the AD7609 ADC from Analog Devices.
- capable of 200kSPS, 16 bits, +/-10V

**Measured Noise** The measurement of the ADC noise was done by short-circuiting its input with a 50 Ohm resistor and recording the digital value at 10kHz. The amplitude spectral density of the recorded values are computed and shown in Figure 3.1. The ADC noise is a white noise with an amplitude spectral density of  $5.6 \mu\text{V}/\sqrt{\text{Hz}}$  (RMS value of 0.4mV), which fulfills the specifications. All ADC channels are measuring the same, so the noise of only one channel is here shown.

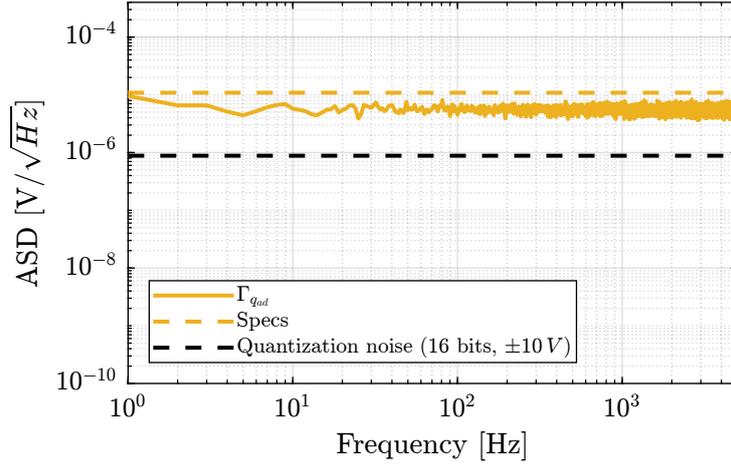
If required, it is possible to apply some oversampling to lower the obtained noise as explained in **lab13'improv'adc**. To have additional  $w$  bits of resolution, the oversampling frequency  $f_{os}$  should be  $f_{os} = 4^w \cdot f_s$ . As the ADC can work at 200kSPS, and the real time controller only runs at 10kSPS, an oversampling factor of 16 can be used to have approximately two more bits of resolution (i.e. reducing the noise by a factor 4). This works because the noise can be approximated by a white noise and the amplitude is larger than 1 LSB (0.3 mV) **hauser91'princ'overs'conver**.

**Reading of piezoelectric force sensor** To further verify that the ADC can effectively measure the voltage generated by a piezoelectric stack without issue, a test with the APA95ML was performed. The setup is shown in Figure 3.2 where two stacks are used as actuator (in parallel) and one stack is used as a sensor. The voltage amplifier used has a gain of 20.

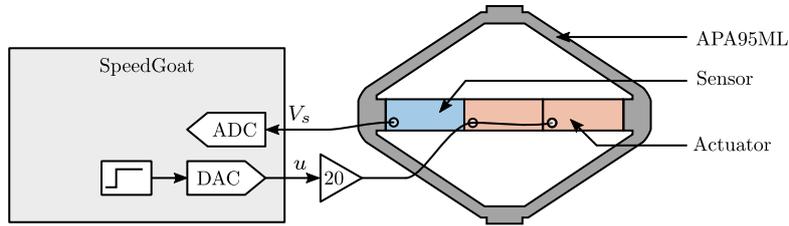
Steps signals was generated using the DAC with an amplitude of 1V, and the ADC signal was recorded. The excitation signal (steps) and measured voltage across the sensor stack are shown in Figure 3.3b.

Two things can be observed:

- an offset voltage of 2.26 V
- the measured voltage shows an exponential decay response to the step input



**Figure 3.1:** Measured ADC noise (IO318)



**Figure 3.2:** Schematic of the setup to validate the use of the ADC for reading the force sensor voltage

This can be understood by the electrical schematic shown in Figure 3.3a were the ADC has some input impedance  $R_i$  and input bias current  $i_n$ .

The input impedance  $R_i$  of the ADC with the capacitance  $C_p$  of the piezoelectric stack sensor forms an RC circuit with a time constant  $\tau = R_i C_p$ . The charge generated by the piezoelectric effects across its capacitance is discharging into the input resistor of the ADC. Therefore, the transfer function from the generated voltage  $V_p$  to the measured voltage  $V_{ADC}$  is a first order high filter, with time constant  $\tau$ . The an exponential curve was fitted to the experimental data and a time constant  $\tau = 6.5 s$  was obtained. With the capacitance of the piezoelectric sensor stack being  $C_p = 4.4 \mu F$ , the internal impedance of the Speedgoat ADC can be computed as follows  $R_i = \frac{\tau}{C_p} = 1.5 M\Omega$ . It is close to the specified value of  $1 M\Omega$  found in the datasheet

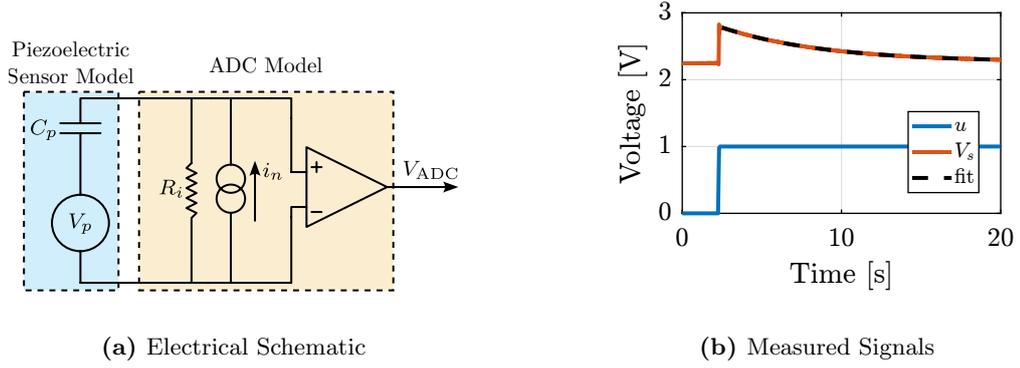
The constant voltage offset can be explained by the input bias current  $i_n$  of the ADC, represented in Figure 3.3a At DC, the impedance of the piezoelectric stack is much larger that the input impedance of the ADC, and therefore the input bias current  $i_n$  passing through the internal resistance  $R_i$  produces a constant voltage offset  $V_{off} = R_i i_n$ . The input bias current  $i_n$  is estimated from  $i_n = V_{off}/R_i = 1.5 \mu A$ .

In order to reduce the input voltage offset and to increase the corner frequency of the high pass filter, a resistor  $R_p$  is added in parallel to the force sensor, as illustrated in Figure 3.4a

It has two effects:

- Reduction of input voltage offset:

$$V_{off} = \frac{R_p R_{in}}{R_p + R_{in}} i_n$$



**Figure 3.3:** Electrical schematic of the ADC measuring the piezoelectric force sensor (a), adapted from `reza06'piezoel'trans'vibrat'contr'dampin`. Measured voltage  $V_s$  while step voltages are generated for the actuator stacks (b).

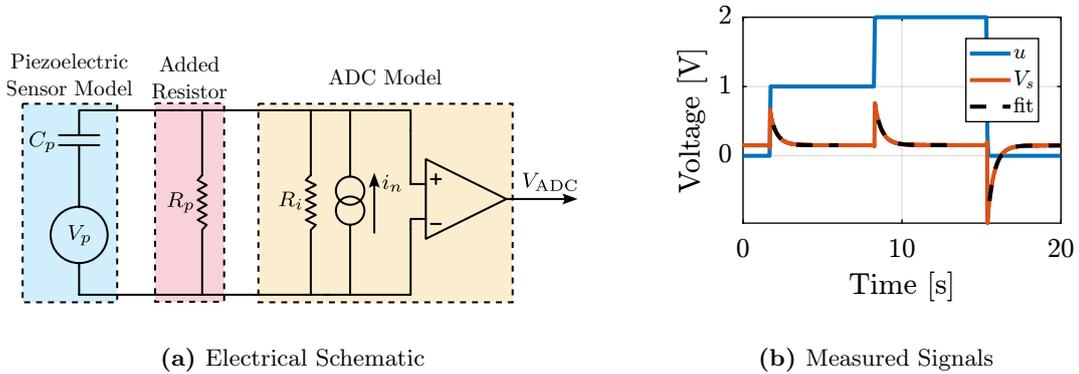
- Increase the high pass corner frequency  $f_c$

$$\frac{R_i R_p}{R_i + R_p} C_p = \tau_c = \frac{1}{2\pi f_c}$$

$$R_p = \frac{R_i}{2\pi f_c C_p R_i - 1}$$

The resistor is chosen such that the high pass corner frequency is equal to 0.5 Hz. This corresponds to a resistor of  $R_p = 76 \text{ k}\Omega$ . With this parallel resistance value, the voltage offset would be  $V_{\text{off}} = 0.11 \text{ V}$ , which is much more acceptable.

To validate this, a resistor  $R_p \approx 82 \text{ k}\Omega$  is then added in parallel with the force sensor as shown in Figure 3.4a. After the resistor is added, the same steps response were performed (Figure 3.4b). And indeed, we obtain a much smaller offset voltage ( $V_{\text{off}} = 0.15 \text{ V}$ ) and a much faster time constant ( $\tau = 0.45 \text{ s}$ ). This validates the model of the ADC and the effectiveness of the added resistor.



**Figure 3.4:** Effect of an added resistor  $R_p$  in parallel to the force sensor. The electrical schematic is shown in (a) and the measured signals in (b).

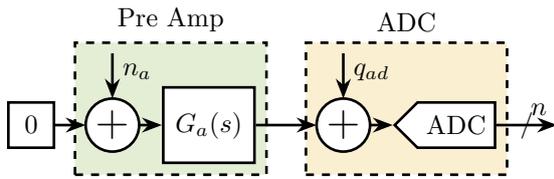
## 3.2 Instrumentation Amplifier

Because the ADC noise may be too large to measure noise of other instruments (anything below  $5.6 \mu V/\sqrt{Hz}$  cannot be distinguish from the noise of the ADC itself), a low noise instrumentation amplifier can be used. Here, a Femto DLPVA-101-B-S amplifier, with gains from 20dB up to 80dB, was used.

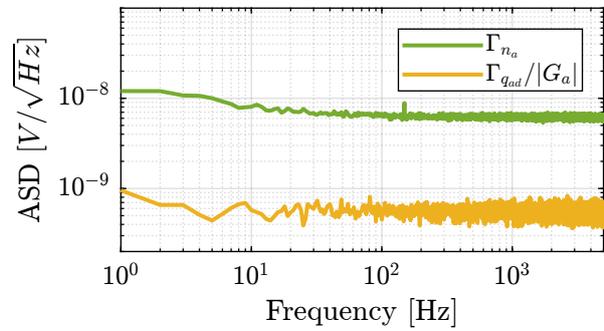
But first, the input<sup>1</sup> noise of the amplifier was characterized. To do so, its input was short circuited with a  $50 \Omega$  resistor, and the output voltage was measured by the ADC (Figure 3.5). The maximum amplifier gain of 80dB (i.e. 10000) was used.

The measured voltage  $n$  was then divided by 10000 to obtain the equivalent noise at the input of the voltage amplifier  $n_a$ . In that case, the noise of the ADC  $q_{ad}$  is negligible, thanks to the high gain used. The obtained amplifier noise ASD  $\Gamma_{n_a}$  and the (negligible) contribution of the ADC noise are shown in Figure 3.6.

It was also verified that the bandwidth of the instrumentation amplifier is much larger than 5kHz such that not phase drop are added by the use of the amplifier in the frequency band of interest.



**Figure 3.5:** Measurement of the instrumentation amplifier input voltage noise



**Figure 3.6:** Obtained ASD of the instrumentation amplifier input voltage noise

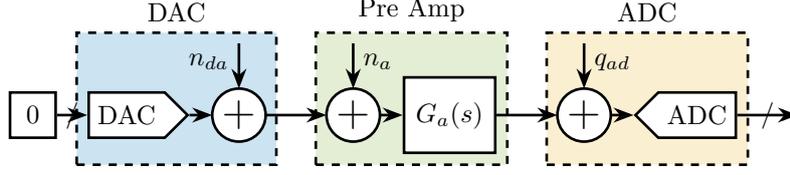
## 3.3 Digital to Analog Converters

**Output Voltage Noise** In order to measure the output noise of the DAC, the measurement setup schematically represented in Figure 3.7 was used. The DAC was instructed to output constant voltage (here zero), and the gain of the pre-amplifier is adjusted such that the measured amplified noise is much larger than the quantization noise of the ADC.

The Amplitude Spectral Density  $\Gamma_{n_{da}}(\omega)$  of the measured signal was computed and it was verified the contribution of the ADC noise and amplifier noise are negligible.

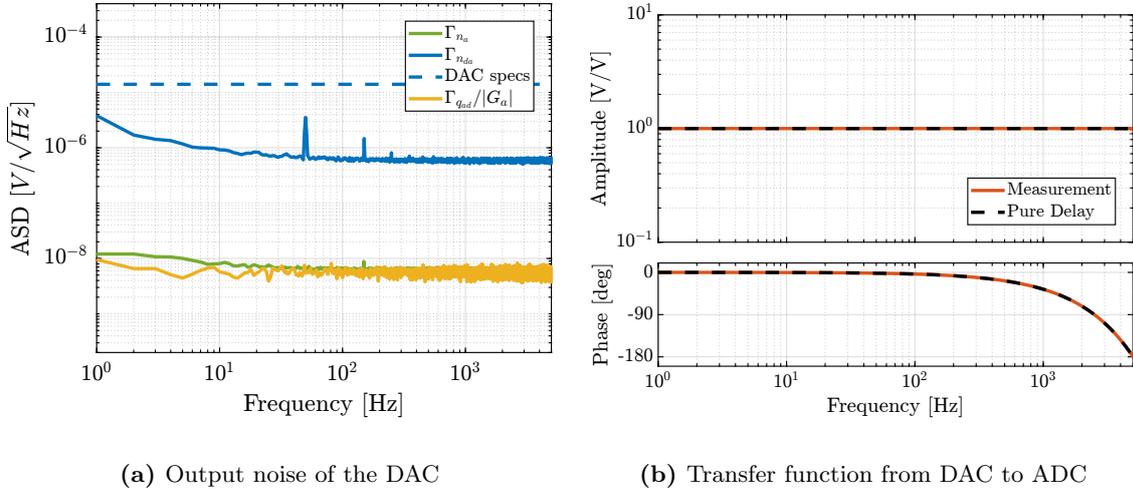
The obtained Amplitude Spectral Density of the DAC's output voltage is shown in Figure 3.8a. It is almost white noise with an ASD of  $0.6 \mu V/\sqrt{Hz}$ . There is a little bit of 50Hz, and some low frequency noise (thermal noise?) which are not foreseen to be an issue as it will be inside the bandwidth. Note that all channels are measuring the same, so only one channel is shown here.

<sup>1</sup>For variable gain amplifiers, it is usual to refer to the input noise rather than the output noise, as the input referred noise is almost independent on the chosen gain.



**Figure 3.7:** Measurement of the DAC output voltage noise. A pre-amplifier with a gain of 1000 is used before measuring the signal with the ADC.

**Delay from ADC to DAC** In order to measure the transfer function from DAC to ADC and verify that the bandwidth of both instrument is high enough, the DAC output was directly wired to the ADC input. A white noise signal was generated by the DAC, and the ADC signal was recorded. The obtained frequency response function from the digital DAC signal to the digital ADC signal is shown in (Figure 3.8b). It corresponds to 1 sample delay, which is corresponding to the specifications.



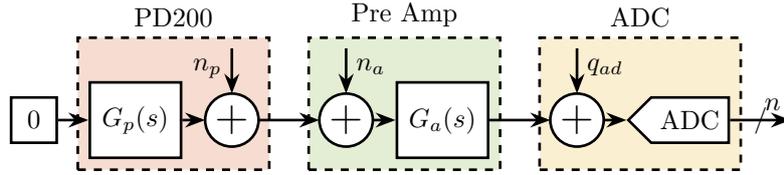
**Figure 3.8:** Measurement of the output voltage noise of the ADC (a) and measured transfer function from DAC to ADC (b) which corresponds to a “1-sample” delay.

### 3.4 Piezoelectric Voltage Amplifier

**Output Voltage Noise** The measurement setup is shown in Figure 3.9. The input of the PD200 amplifier is shunted with a  $50\ \Omega$  resistor such that only the noise of the amplifier itself is measured. The gain of the pre-amplifier was increased in order to measure a signal much larger than the noise of the ADC. Two piezoelectric stacks of the APA95ML were connected to the PD200 output to provide an appropriate load.

The Amplitude Spectral Density  $\Gamma_n(\omega)$  of the measured signal by the ADC is computed. The Amplitude Spectral Density of the output voltage noise of the PD200 amplifier  $n_p$  is then computed taking into account the gain of the pre-amplifier:

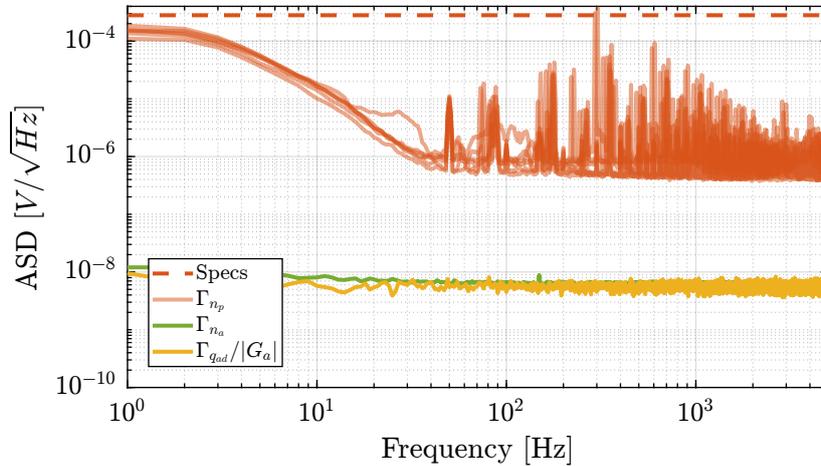
$$\Gamma_{n_p}(\omega) = \frac{\Gamma_n(\omega)}{|G_p(j\omega)G_a(j\omega)|} \quad (3.1)$$



**Figure 3.9:** Setup used to measured the output voltage noise of the PD200 voltage amplifier. A gain  $G_a = 1000$  was used for the instrumentation amplifier.

The Amplitude Spectral Density of the measured output noise of the PD200 is computed and shown in Figure 3.10. It is verified that the contribution of the PD200 noise is much larger than the contribution of the pre-amplifier noise of the quantization noise (i.e. what is measured is indeed the PD200 noise). Here, the measured noise of the six received amplifiers are all shown.

The Amplitude Spectral Density of the output voltage noise of the PD200 amplifiers present sharp peaks. The reason for all these peaks is not clear, but as their amplitude are bellow the specifications, it should not pose any issue.



**Figure 3.10:** Measured output voltage noise of the PD200 amplifiers

**Small Signal Bandwidth** Here the small signal dynamics of all the PD200 amplifiers are identified.

A (logarithmic) sweep sine excitation voltage is generated by the Speedgoat DAC with an amplitude of 0.1V and a frequency going from 1Hz up to 5kHz.

The output voltage of the PD200 amplifier is measured thanks to the monitor voltage of the PD200 amplifier. The input voltage of the PD200 amplifier (the generated voltage by the DAC) is measured with another ADC of the Speedgoat. This way, the time delay related to the ADC will not be apparent in the results.

All six received amplifiers are measuring the same regarding their transfer functions. The amplitude is constant over a wide frequency band and the phase drop is limited to less than 1 degree up to 500Hz, which is well within the specifications.

The identified dynamics in Figure 3.11 can very well be modeled with a first order low pass filter or

even a simple constant.

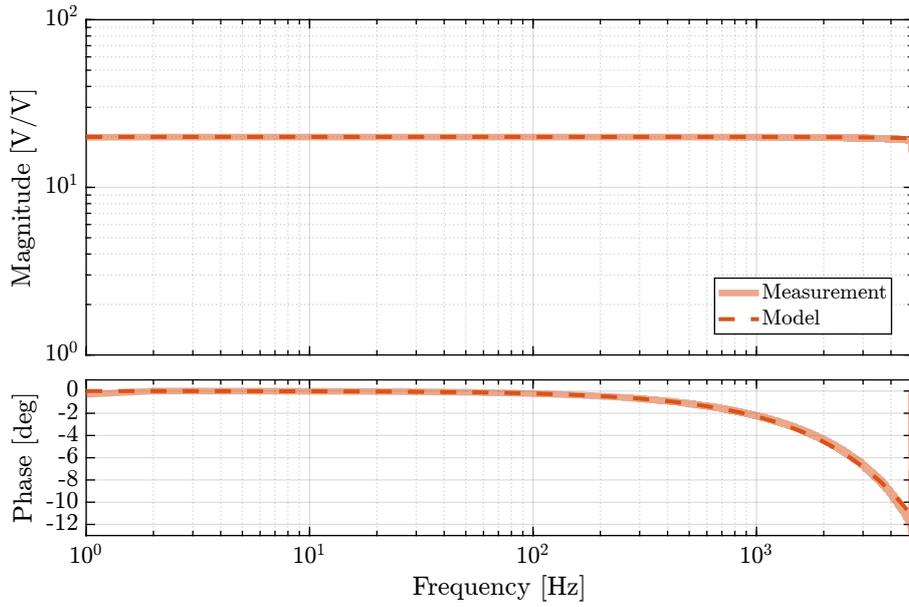


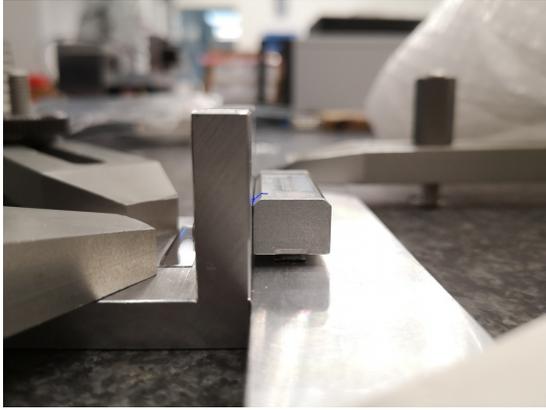
Figure 3.11: Identified dynamics from input voltage to output voltage

### 3.5 Linear Encoders

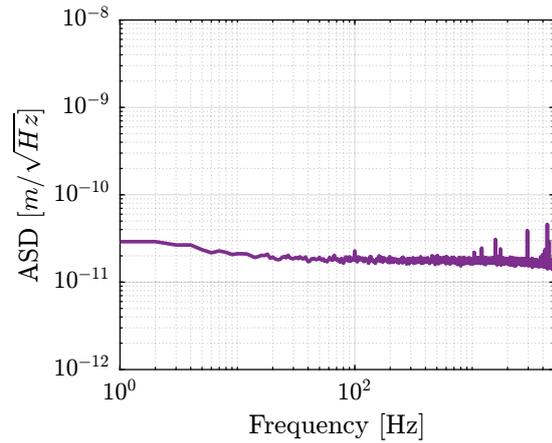
To measure the noise  $n$  of the encoder, one can rigidly fix the head and the ruler together such that no motion should be measured. Then, the measured signal  $y_m$  corresponds to the noise  $n$ .

The measurement bench is shown in Figure 3.12. Note that the bench is then covered with a “plastic bubble sheet” in order to keep disturbances as small as possible. Then, and for all the six encoders, the measured motion during 100s with a sampling frequency of 20kHz.

The obtained amplitude spectral density of the measured displacement (i.e. measurement noise) is shown in Figure 3.13. It corresponds to a white noise, with an amplitude  $\approx 1\text{ nm RMS}$ .



**Figure 3.12:** Test bench used to measured the encoder noise



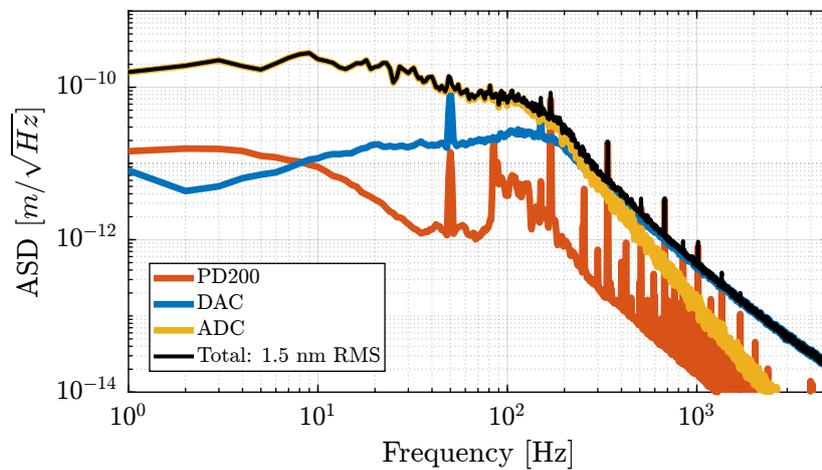
**Figure 3.13:** Measured Amplitude Spectral Density of the encoder noise

### 3.6 Noise budgeting from measured instrumentation noise

Once all the instrumentation noise were characterized, the effect of the instrumentation noise on the sample's vibration can be assessed using the multi-body model.

The obtained vertical motion induced by the ADC noise, DAC noise and voltage amplifier noise is displayed in Figure 3.14 (the effect of encoder noise is negligible).

The total motion induced by all the noise sources is around  $1.5\text{ nm}$  which is well within the specifications.



**Figure 3.14:** Closed-loop noise budgeting using measured noise of instrumentation

# Conclusion

- thanks to multi-body model in which it is easy to include instrumentation and noise sources From specification on the sample's vertical motion (most stringent requirement), specification for each noise source was extracted.
- based on those specifications, adequate instrumentation were chosen. for some instrumentation, it was difficult to choose only based on data-sheets are manufacturers often don't share relevant information for noise budgets, such as amplitude spectral densities
- then, the instrumentation was procured and tested individually. All were found to comply with the requirements. Finally, based on the measured noise of all instrumentation, the expected sample's vibration induced by all the noise sources was estimated and found to comply with the requirements.