Nano Active Stabilization System - Instrumentation

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This chapter presents a systematic approach to selecting and validating appropriate instrumentation for the nano active stabilization system (NASS), ensuring each component meets specific performance requirements. Figure 1 illustrates the control diagram with all relevant noise sources whose effects on sample position will be evaluated throughout this analysis.

The selection process follows a three-stage methodology. First, dynamic error budgeting is performed in Section 1 to establish maximum acceptable noise specifications for each instrumentation component (ADC, DAC, and voltage amplifier). This analysis employs the multi-body model with a 2DoF APA model, focusing particularly on the vertical direction due to its more stringent requirements. From the calculated transfer functions, maximum acceptable amplitude spectral densities for each noise source are derived.

Section 2 then presents the selection of appropriate components based on these noise specifications and additional requirements.

Finally, Section 3 validates the selected components through experimental testing. Each instrument is characterized individually, measuring actual noise levels and performance characteristics. The measured noise characteristics are then incorporated into the multi-body model to confirm that the combined effect of all instrumentation noise sources remains within acceptable limits.

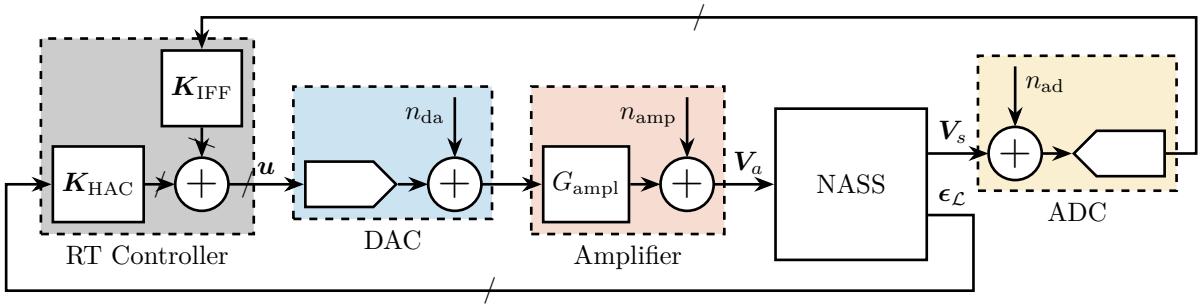


Figure 1: Block diagram of the NASS with considered instrumentation. The RT controller is a Speedgoat machine.

1 Dynamic Error Budgeting

The primary goal of this analysis is to establish specifications for the maximum allowable noise levels in the instrumentation used for the NASS (ADC, DAC, and voltage amplifier) that would result in acceptable vibration levels in the system.

The procedure involves determining the closed-loop transfer functions from various noise sources to positioning error (Section 1.1). This analysis is conducted using the multi-body model with a 2-DoF Amplified Piezoelectric Actuator model that incorporates voltage inputs and outputs. Only the vertical direction is considered in this analysis as it presents the most stringent requirements; the horizontal directions are subject to less demanding constraints.

From these transfer functions, the maximum acceptable Amplitude Spectral Density (ASD) of the noise sources is derived (Section 1.2). Since the voltage amplifier gain affects the amplification of DAC noise, an assumption of an amplifier gain of 20 was made.

1.1 Closed-Loop Sensitivity to Instrumentation Disturbances

Several key noise sources are considered in the analysis (Figure 1). These include the output voltage noise of the DAC (n_{da}), the output voltage noise of the voltage amplifier (n_{amp}), and the voltage noise of the ADC measuring the force sensor stacks (n_{ad}).

Encoder noise, which is only used to estimate R_z, has been found to have minimal impact on the vertical sample error and is therefore omitted from this analysis for clarity.

The transfer functions from these three noise sources (for one strut) to the vertical error of the sample are estimated from the multi-body model, which includes the APA300ML and the designed flexible joints (Figure 1.1).

1.2 Estimation of maximum instrumentation noise

From the previous analysis, the relationship between the noise of the instrumentation and its effect on the vertical error of the sample as a function of frequency has been established. The next step involves determining specifications for each instrumentation component to ensure that the effect on the vertical error of the sample remains within acceptable limits.

The most stringent requirement for the system is maintaining vertical vibrations below the smallest expected beam size of 100 nm, which corresponds to a maximum allowed vibration of 15 nm RMS.

Several assumptions regarding the noise characteristics have been made. The DAC, ADC, and amplifier noise are considered uncorrelated, which is a reasonable assumption. Similarly, the noise corresponding

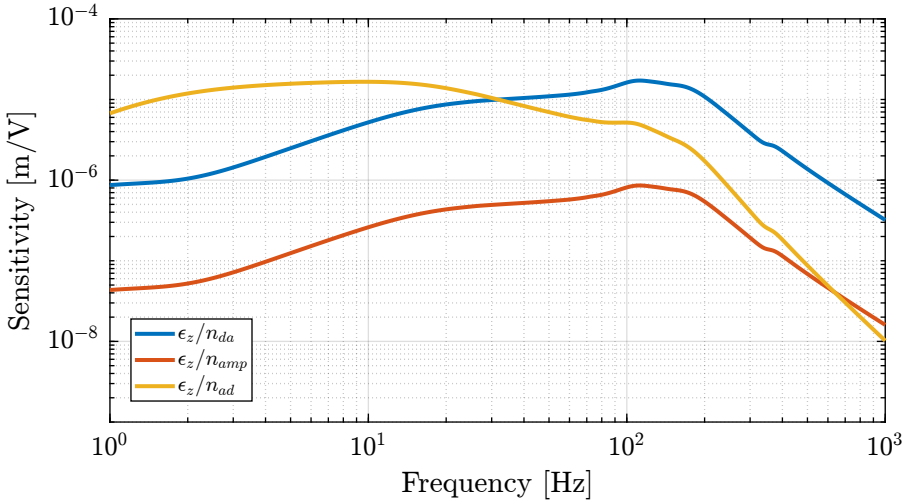


Figure 1.1: Transfer function from noise sources to vertical motion errors

to each strut is assumed to be uncorrelated. This means that the power spectral densities (PSD) of the different noise sources can be summed.

The system symmetry has been utilized to simplify the analysis. The effect of all struts on the vertical errors is identical, as verified from the extracted sensitivity curves. Therefore, only one strut is considered for this analysis, and the total effect of the six struts is calculated as six times the effect of one strut in terms of power, which translates to a factor of $\sqrt{6} \approx 2.5$ for RMS values.

In order to derive specifications in terms of noise spectral density for each instrumentation component, a white noise profile is assumed, which is typical for these components.

The noise specification is computed such that if all instrumentation components operate at their maximum allowable noise levels, the specification for vertical error will still be met. While this represents a pessimistic approach, it provides a reasonable estimate of the required specifications.

Based on this analysis, the obtained maximum noise levels are as follows: DAC maximum output noise ASD is established at $14\,\mu V/\sqrt{\text{Hz}}$, voltage amplifier maximum output voltage noise ASD at $280\,\mu V/\sqrt{\text{Hz}}$, and ADC maximum measurement noise ASD at $11\,\mu V/\sqrt{\text{Hz}}$. In terms of RMS noise, these translate to less than 1 mV RMS for the DAC, less than 20 mV RMS for the voltage amplifier, and less than 0.8 mV RMS for the ADC.

If the Amplitude Spectral Density of the noise of the ADC, DAC, and voltage amplifiers all remain below these specified maximum levels, then the induced vertical error will be maintained below 15nm RMS. These specifications will guide the selection of appropriate instrumentation in Section 2.

2 Choice of Instrumentation

The selection of appropriate instrumentation components was based on the noise specifications derived in Section 1 and other relevant specifications that will be further developed.

This section presents the evaluation process for ADCs, DACs, voltage amplifiers, and relative positioning sensors, detailing the comparison between different options and justifying the final selections.

2.1 Piezoelectric Voltage Amplifier

Several characteristics of piezoelectric voltage amplifiers must be considered for this application. To utilize the full stroke of the piezoelectric actuator, the voltage output should range between -20 and $150\,V$. The amplifier should accept an analog input voltage, preferably in the range of -10 to $10\,V$, as this is standard for most DACs.

Small signal Bandwidth and Output Impedance Two distinct bandwidth specifications are relevant for piezoelectric voltage amplifiers: large signal bandwidth and small signal bandwidth. Large signal bandwidth relates to the output current capabilities of the amplifier and will be discussed in the next section.

Small signal bandwidth is particularly important for feedback applications as it can limit the overall bandwidth of the complete feedback system.

A simplified electrical model of a voltage amplifier connected to a piezoelectric stack is shown in Figure 2.1. This model is valid for small signals and provides insight into the small signal bandwidth limitation [1, chap. 14]. In this model, R_o represents the output impedance of the amplifier. When combined with the piezoelectric load (represented as a capacitance C_p), it forms a first order low pass filter described by equation 2.1.

$$\frac{V_a}{V_i}(s) = \frac{1}{1 + \frac{s}{\omega_0}}, \quad \omega_0 = \frac{1}{R_o C_p} \tag{2.1}$$

Consequently, the small signal bandwidth depends on the load capacitance and decreases as the load capacitance increases. For the APA300ML, the capacitive load of the two piezoelectric stacks corresponds to $C_p = 8.8\,\mu F$. If a small signal bandwidth of $f_0 = \frac{\omega_0}{2\pi} = 5\,\text{kHz}$ is desired, the voltage amplifier output impedance should be less than $R_0 = 3.6\,\Omega$.

Large signal Bandwidth Large signal bandwidth relates to the maximum output capabilities of the amplifier in terms of amplitude as a function of frequency.

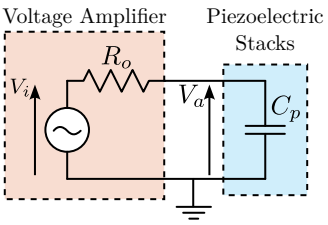


Figure 2.1: Electrical model of a voltage amplifier with output impedance R_0 connected to a piezoelectric stack with capacitance C_p

Since the primary function of the NASS is position stabilization rather than scanning, this specification is less critical than the small signal bandwidth. However, considering potential scanning capabilities, a worst-case scenario of a constant velocity scan (triangular reference signal) with a repetition rate of $f_r = 100\,\text{Hz}$ using the full voltage range of the piezoelectric actuator ($V_{pp} = 170\,V$) is considered.

There are two limiting factors for large signal bandwidth that should be evaluated:

1. Slew rate, which should exceed $2 \cdot V_{pp} \cdot f_r = 34\,V/ms$. This requirement is typically easily met by commercial voltage amplifiers.

2. Current output capabilities: as the capacitive impedance decreases inversely with frequency, it can reach very low values at high frequencies. To achieve high voltage at high frequency, the amplifier must provide substantial current. The maximum required current can be calculated as $I_{\max} = 2 \cdot V_{pp} \cdot f \cdot C_p = 0.3\,A$.

Therefore, ideally, a voltage amplifier capable of providing $0.3\,A$ of current is needed.

Output voltage noise As established in Section 1, the output noise of the voltage amplifier should be below 20 mV RMS.

It should be noted that the load capacitance of the piezoelectric stack filters the output noise of the amplifier, as illustrated by the low pass filter in Figure 2.1. Therefore, when comparing noise specifications from different voltage amplifier datasheets, it is essential to verify the capacitance of the load used in the measurement (i.e., the low signal bandwidth considered) [2].

For this application, the output noise must remain below 20 mV RMS with a load of $8.8\,\mu F$ and a bandwidth exceeding 5 kHz.

Choice of voltage amplifier The specifications are summarized in Table 2.1. The most critical characteristics are the small signal bandwidth ($> 5\,\text{kHz}$) and the output voltage noise ($< 20\,\text{mV}$ RMS).

Several voltage amplifiers were considered, with their datasheet information presented in Table 2.1. One challenge encountered during the selection process was that manufacturers typically do not specify output noise as a function of frequency (i.e., the ASD of the noise), but instead provide only the RMS value, which represents the integrated value across all frequencies. This approach does not account for the frequency dependency of the noise, which is crucial for accurate error budgeting.

Additionally, the load conditions used to estimate bandwidth and noise specifications are often not explicitly stated. In many cases, bandwidth is reported with minimal load while noise is measured with

substantial load, making direct comparisons between different models more complex.

The PD200 from PiezoDrive was ultimately selected because it meets all the requirements and is accompanied by clear documentation, particularly regarding noise characteristics and bandwidth specifications.

Table 2.1: Specifications for the Voltage amplifier and considered commercial products

Specification	**PD200** PiezoDrive	WMA-200 Falco	LA75B Cedrat	E-505 PI
Input Voltage Range: $\pm 10\,V$	$\pm 10\,V$	$\pm 8.75\,V$	$-1/7.5\,V$	
Output Voltage Range: $-20/150\,V$	$-50/150\,V$	$\pm 175\,V$	$-20/150\,V$	-30/130
Gain > 15	20	20	20	10
Output Current $> 300\,mA$	$900\,mA$	$150\,mA$	$360\,mA$	$215\,mA$
Slew Rate $> 34\,V/ms$	$150\,V/\mu s$	$80\,V/\mu s$	n/a	n/a
Output noise $< 20\,mV$ RMS	$0.7\,mV$ RMS	$0.05\,mV$	$3.4\,mV$	$0.6\,mV$
(10uF load)	($10\,\mu F$ load)	($10\,\mu F$ load)	(n/a)	(n/a)
Small Signal Bandwidth $> 5\,kHz$	$6.4\,kHz$	$300\,Hz$	$30\,kHz$	n/a
($10\,\mu F$ load)	($10\,\mu F$ load)	[1]	(unloaded)	(n/a)
Output Impedance: $< 3.6\,\Omega$	n/a	$50\,\Omega^{??}$	n/a	n/a

2.2 ADC and DAC

Analog-to-digital converters and digital-to-analog converters play key roles in the system, serving as the interface between the digital RT controller and the analog physical plant. The proper selection of these components is critical for system performance.

Synchronicity and Jitter For control systems, synchronous sampling of inputs and outputs of the real-time controller and minimal jitter are essential requirements. These factors significantly impact control performance, as highlighted in [3], [4].

Therefore, the ADC and DAC must be well interfaced with the Speedgoat real-time controller and triggered synchronously with the computation of the control signals. Based on this requirement, priority was given to ADC and DAC components specifically marketed by Speedgoat to ensure optimal integration.

Sampling Frequency, Bandwidth and delays Several requirements that may initially appear similar are actually distinct in nature.

First, the *sampling frequency* defines the interval between two sampled points and determines the Nyquist frequency. Then, the *bandwidth* specifies the maximum frequency of a measured signal (typically defined as the -3dB point) and is often limited by implemented anti-aliasing filters. Finally, *delay* (or *latency*) refers to the time interval between the analog signal at the input of the ADC and the digital information transferred to the control system.

[1] The manufacturer proposed to remove the $50\,\Omega$ output resistor to improve to small signal bandwidth above $10\,kHz$

Sigma-Delta ADCs can provide excellent noise characteristics, high bandwidth, and sampling frequency, but often at the cost of poor latency. Typically, the latency can reach 20 times the sampling period [5, chapt. 8.4]. Consequently, while Sigma-Delta ADCs are widely used for signal acquisition applications, they have limited utility in real-time control scenarios where latency is a critical factor.

For real-time control applications, SAR-ADCs (Successive Approximation ADCs) remain the predominant choice due to their single-sample latency characteristics.

ADC Noise Based on the dynamic error budget established in Section 1, the measurement noise ASD should not exceed $11\,\mu V/\sqrt{\text{Hz}}$, equivalent to 0.8 mV RMS.

ADCs are subject to various noise sources. Quantization noise, which results from the discrete nature of digital representation, is one of these sources. To determine the minimum bit depth required to meet the noise specifications, the quantization noise must be analyzed.

Assuming an ideal ADC where quantization error is the only noise source, the quantization step size, denoted as $q = \Delta V/2^n$, represents the voltage equivalent of the least significant bit. Here, ΔV is the full range of the ADC in volts, n is the bit depth, and F_s is the sampling frequency in Hertz.

The quantization noise ranges between $\pm q/2$, and its probability density function is constant across this range (uniform distribution). Since the integral of this probability density function $p(e)$ equals one, its value is $1/q$ for $-q/2 < e < q/2$, as illustrated in Figure 2.2.

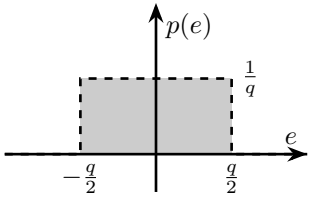


Figure 2.2: Probability density function $p(e)$ of the ADC error e

The variance (or time-average power) of the quantization noise is expressed by equation 2.2:

$$P_q = \int_{-q/2}^{q/2} e^2 p(e) de = \frac{q^2}{12} \tag{2.2}$$

To compute the power spectral density of the quantization noise, which is defined as the Fourier transform of the noise's autocorrelation function, it is assumed that noise samples are uncorrelated. Under this assumption, the autocorrelation function approximates a delta function in the time domain. Since the Fourier transform of a delta function equals one, the power spectral density becomes frequency-independent (white noise).

By Parseval's theorem, the power spectral density of the quantization noise Φ_q can be linked to the ADC sampling frequency and quantization step size (2.3).

$$\int_{-F_s/2}^{F_s/2} \Phi_q(f) df = \int_{-q/2}^{q/2} e^2 p(e) de \quad \Longrightarrow \quad \Phi_q = \frac{q^2}{12F_s} = \frac{\left(\frac{\Delta V}{2^n}\right)^2}{12F_s} \quad \text{in} \quad \left[\frac{V^2}{\text{Hz}}\right] \tag{2.3}$$

From a specified noise amplitude spectral density $\Gamma_{\max}$, the minimum number of bits required to keep quantization noise below $\Gamma_{\max}$ is calculated using equation 2.4.

$$n = \log_2 \left(\frac{\Delta V}{\sqrt{12 F_s} \cdot \Gamma_{\max}} \right) \tag{2.4}$$

With a sampling frequency $F_s = 10\,\text{kHz}$, an input range $\Delta V = 20\,V$ and a maximum allowed ASD $\Gamma_{\max} = 11\,\mu V/\sqrt{Hz}$, the minimum number of bits is $n_{\min} = 12.4$, which is readily achievable with commercial ADCs.

DAC Output voltage noise Similar to the ADC requirements, the DAC output voltage noise ASD should not exceed $14\,\mu V/\sqrt{Hz}$, equivalent to 1 mV RMS. This specification corresponds to a 13-bit $\pm 10\,V$ DAC, which is easily attainable with current technology.

Choice of the ADC and DAC Board Based on the preceding analysis, the selection of suitable ADC and DAC components is straightforward.

For optimal synchronicity, a Speedgoat-integrated solution was chosen. The selected model is the IO131, which features 16 analog inputs based on the AD7609 with 16-bit resolution, $\pm 10\,V$ range, maximum sampling rate of 200kSPS, simultaneous sampling, and differential inputs allowing the use of shielded twisted pairs for enhanced noise immunity. The board also includes 8 analog outputs based on the AD5754R with 16-bit resolution, $\pm 10\,V$ range, conversion time of $10\,\mu s$, and simultaneous update capability.

Although noise specifications are not explicitly provided in the datasheet, the 16-bit resolution should ensure performance well below the established requirements. This will be experimentally verified in Section 3.

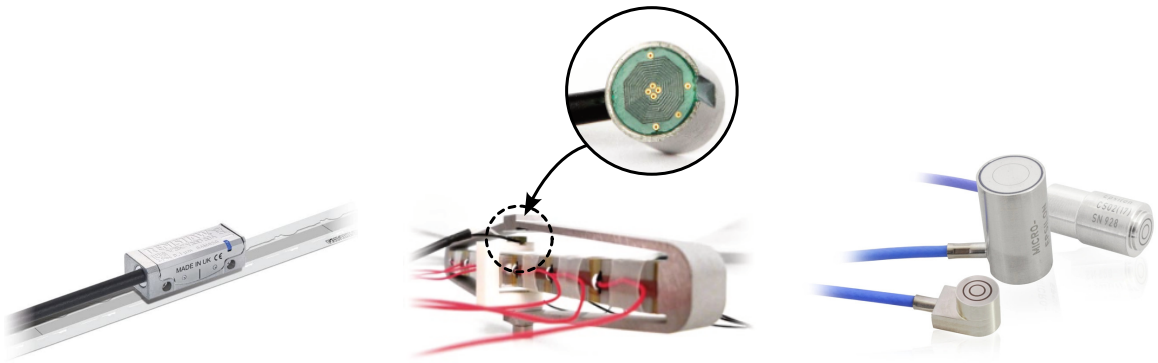
2.3 Relative Displacement Sensors

The specifications for the relative displacement sensors include sufficient compactness for integration within each strut, noise levels below 6 nm RMS (derived from the 15 nm RMS vertical error requirement for the system divided by the contributions of six struts), and a measurement range exceeding $100\,\mu m$.

Several sensor technologies are capable of meeting these requirements [6]. These include optical encoders (Figure 2.3a), capacitive sensors (Figure 2.3c), and eddy current sensors (Figure 2.3b), each with their own advantages and implementation considerations.

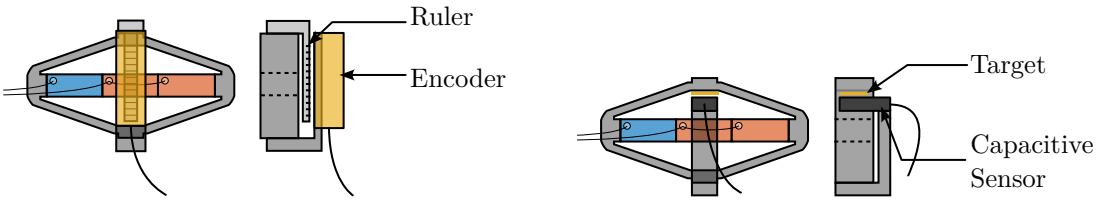
From an implementation perspective, capacitive and eddy current sensors offer a slight advantage as they can be quite compact and can measure in line with the APA, as illustrated in Figure 2.4b. In contrast, optical encoders are bigger and they must be offset from the strut's action line, which introduces potential measurement errors (Abbe errors) due to relative rotations between the two ends of the APA, as shown in Figure 2.4a.

A significant consideration in the sensor selection process was the fact that sensor signals must pass through an electrical slip-ring due to the continuous spindle rotation. Measurements conducted on the



(a) Optical Linear Encoder **(b)** Eddy Current Sensor **(c)** Capacitive Sensor

Figure 2.3: Relative motion sensors considered for measuring the nano-hexapod strut motion



(a) Optical Encoder **(b)** Capacitive Sensor

Figure 2.4: Implementation of relative displacement sensor to measure the motion of the APA

slip-ring integrated in the micro-station revealed substantial cross-talk between different slip-ring channels. To mitigate this issue, preference was given to sensors that transmit displacement measurements digitally, as these are inherently less susceptible to noise and cross-talk. Based on this criterion, an optical encoder with digital output was selected, where signal interpolation is performed directly in the sensor head.

The specifications of the considered relative motion sensor, the Renishaw Vionic, are summarized in Table 2.2, alongside alternative options that were considered.

Table 2.2: Characteristics of the Vionic compared with the specifications

Specification	**Renishaw Vionic**	LION CPL190	Cedrat ECP500
Technology	Digital Encoder	Capacitive	Eddy Current
Bandwidth $> 5\,\text{kHz}$	$> 500\,\text{kHz}$	10kHz	20kHz
Noise $< 6\,nm\,\text{RMS}$	1.6 nm rms	4 nm rms	15 nm rms
Range $> 100\,\mu m$	Ruler length	250 um	500um
In line measurement		×	×
Digital Output	×		

3 Characterization of Instrumentation

Following the procurement of all instrumentation components, individual testing was conducted to verify their compliance with the specified requirements.

3.1 Analog to Digital Converters

Measured Noise The measurement of ADC noise was performed by short-circuiting its input with a 50 Ω resistor and recording the digital values at a sampling rate of 10 kHz. The amplitude spectral density of the recorded values was computed and is presented in Figure 3.1. The ADC noise exhibits characteristics of white noise with an amplitude spectral density of $5.6\,\mu V/\sqrt{\text{Hz}}$ (equivalent to 0.4 mV RMS), which satisfies the established specifications. All ADC channels demonstrated similar performance, so only one channel's noise profile is shown.

If necessary, oversampling can be applied to further reduce the noise [7]. To gain w additional bits of resolution, the oversampling frequency f_{os} should be set to $f_{os} = 4^w \cdot F_s$. Given that the ADC can operate at 200kSPS while the real-time controller runs at 10kSPS, an oversampling factor of 16 can be employed to gain approximately two additional bits of resolution (reducing noise by a factor of 4). This approach is effective because the noise approximates white noise and its amplitude exceeds 1 LSB (0.3 mV) [8].

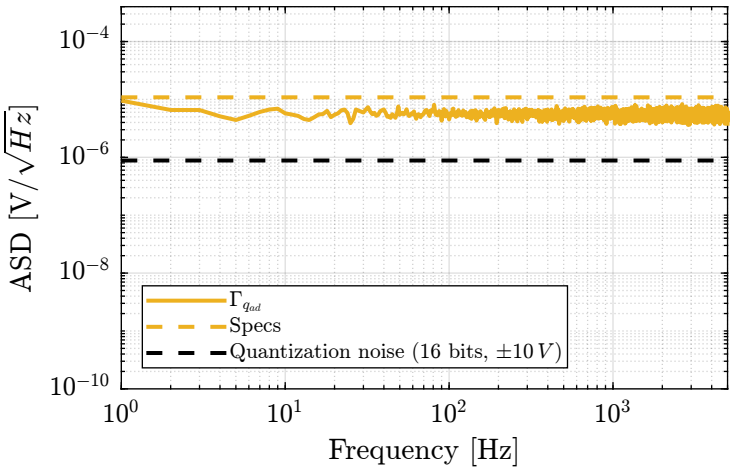


Figure 3.1: Measured ADC noise (IO318)

Reading of piezoelectric force sensor To further validate the ADC's capability to effectively measure voltage generated by a piezoelectric stack, a test was conducted using the APA95ML. The setup is illustrated in Figure 3.2, where two stacks are used as actuators (connected in parallel) and one stack serves as a sensor. The voltage amplifier employed in this setup has a gain of 20.

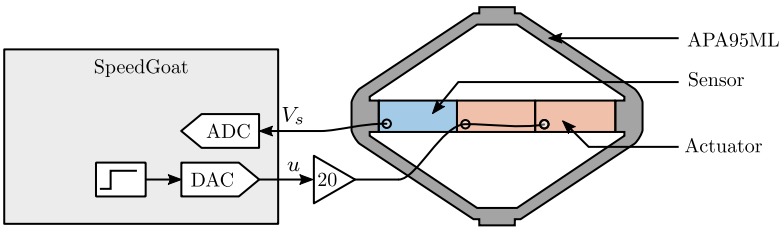


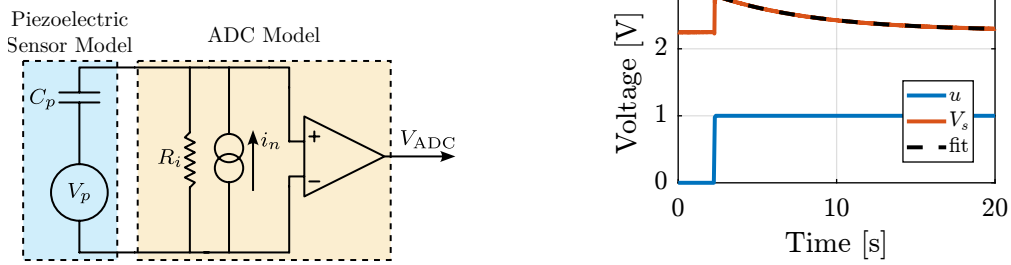
Figure 3.2: Schematic of the setup to validate the use of the ADC for reading the force sensor volage

Step signals with an amplitude of $1\,V$ were generated using the DAC, and the ADC signal was recorded. The excitation signal (steps) and the measured voltage across the sensor stack are displayed in Figure 3.3b.

Two notable observations were made: an offset voltage of $2.26\,V$ was present, and the measured voltage exhibited an exponential decay response to the step input. These phenomena can be explained by examining the electrical schematic shown in Figure 3.3a, where the ADC has an input impedance R_i and an input bias current i_n.

The input impedance R_i of the ADC, in combination with the capacitance C_p of the piezoelectric stack sensor, forms an RC circuit with a time constant $\tau = R_i C_p$. The charge generated by the piezoelectric effect across the stack's capacitance gradually discharges into the input resistor of the ADC. Consequently, the transfer function from the generated voltage V_p to the measured voltage V_{ADC} is a first-order high-pass filter with the time constant τ.

An exponential curve was fitted to the experimental data, yielding a time constant $\tau = 6.5\,s$. With the capacitance of the piezoelectric sensor stack being $C_p = 4.4\,\mu F$, the internal impedance of the Speedgoat ADC was calculated as $R_i = \tau / C_p = 1.5\,M\Omega$, which closely aligns with the specified value of $1\,M\Omega$ found in the datasheet.



(a) Electrical Schematic

(b) Measured Signals

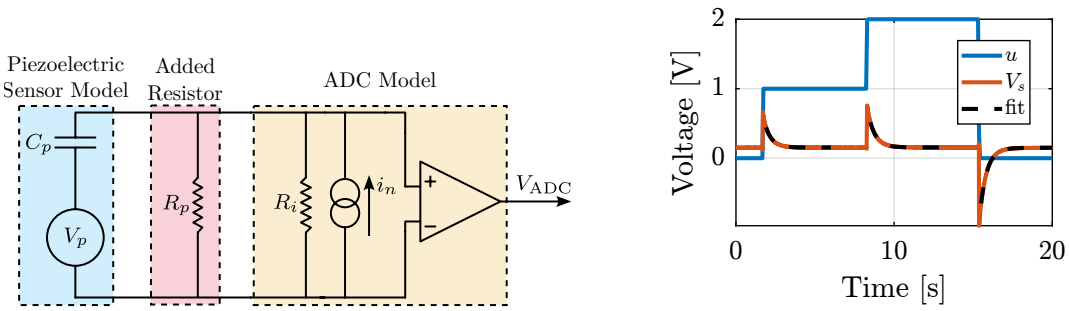
Figure 3.3: Electrical schematic of the ADC measuring the piezoelectric force sensor (a), adapted from [9]. Measured voltage V_s while step voltages are generated for the actuator stacks (b).

The constant voltage offset can be explained by the input bias current i_n of the ADC, represented in Figure 3.3a. At DC, the impedance of the piezoelectric stack is much larger than the input impedance of the ADC, and therefore the input bias current i_n passing through the internal resistance R_i produces a constant voltage offset $V_{\text{off}} = R_i \cdot i_n$. The input bias current i_n is estimated from $i_n = V_{\text{off}} / R_i = 1.5 \mu A$.

In order to reduce the input voltage offset and to increase the corner frequency of the high pass filter, a resistor R_p can be added in parallel to the force sensor, as illustrated in Figure 3.4a. This modification

produces two beneficial effects: a reduction of input voltage offset through the relationship $V_{\text{off}} = (R_p R_i)/(R_p + R_i) i_n$, and an increase in the high pass corner frequency f_c according to the equations $\tau = 1/(2\pi f_c) = (R_i R_p)/(R_i + R_p) C_p$.

To validate this approach, a resistor $R_p \approx 82\,k\Omega$ was added in parallel with the force sensor as shown in Figure 3.4a. After incorporating this resistor, the same step response tests were performed, with results displayed in Figure 3.4b. The measurements confirmed the expected improvements, with a substantially reduced offset voltage ($V_{\text{off}} = 0.15\,V$) and a much faster time constant ($\tau = 0.45\,s$). These results validate both the model of the ADC and the effectiveness of the added parallel resistor as a solution.



(a) Electrical Schematic

(b) Measured Signals

Figure 3.4: Effect of an added resistor R_p in parallel to the force sensor. The electrical schematic is shown in (a) and the measured signals in (b).

3.2 Instrumentation Amplifier

Because the ADC noise may be too low to measure the noise of other instruments (anything below $5.6\,\mu V/\sqrt{\text{Hz}}$ cannot be distinguished from the noise of the ADC itself), a low noise instrumentation amplifier was employed. A Femto DLPVA-101-B-S amplifier with adjustable gains from 20dB up to 80dB was selected for this purpose.

The first step was to characterize the input[1] noise of the amplifier. This was accomplished by short-circuiting its input with a $50\,\Omega$ resistor and measuring the output voltage with the ADC (Figure 3.5). The maximum amplifier gain of 80dB (equivalent to 10000) was utilized for this measurement.

The measured voltage n was then divided by 10000 to determine the equivalent noise at the input of the voltage amplifier n_a. In this configuration, the noise contribution from the ADC q_{ad} is rendered negligible due to the high gain employed. The resulting amplifier noise amplitude spectral density Γ_{n_a} and the (negligible) contribution of the ADC noise are presented in Figure 3.6.

Additionally, verification was performed to ensure that the bandwidth of the instrumentation amplifier significantly exceeds 5kHz, thereby preventing any phase distortion within the frequency band of interest.

[1] For variable gain amplifiers, it is usual to refer to the input noise rather than the output noise, as the input referred noise is almost independent on the chosen gain.

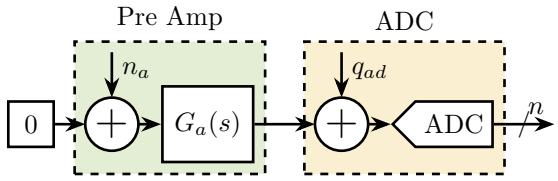


Figure 3.5: Measurement of the instrumentation amplifier input voltage noise

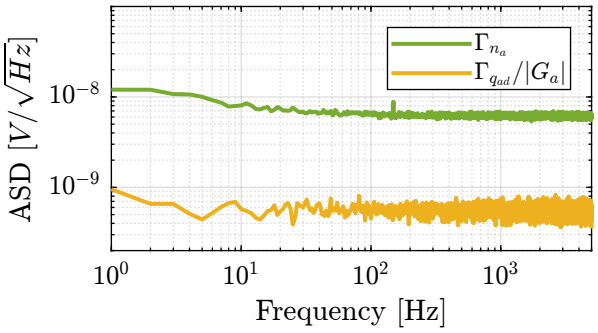


Figure 3.6: Obtained ASD of the instrumentation amplifier input voltage noise

3.3 Digital to Analog Converters

Output Voltage Noise To measure the output noise of the DAC, the setup schematically represented in Figure 3.7 was utilized. The DAC was configured to output a constant voltage (zero in this case), and the gain of the pre-amplifier was adjusted such that the measured amplified noise was significantly larger than the quantization noise of the ADC.

The Amplitude Spectral Density $\Gamma_{n_{da}}(\omega)$ of the measured signal was computed, and verification was performed to confirm that the contributions of ADC noise and amplifier noise were negligible in the measurement.

The resulting Amplitude Spectral Density of the DAC's output voltage is displayed in Figure 3.8a. The noise profile is predominantly white with an ASD of $0.6\,\mu V/\sqrt{\text{Hz}}$. Minor 50 Hz noise is present, along with some low frequency $1/f$ noise, but these are not expected to pose issues as they are well within specifications. It should be noted that all DAC channels demonstrated similar performance, so only one channel's results are presented.

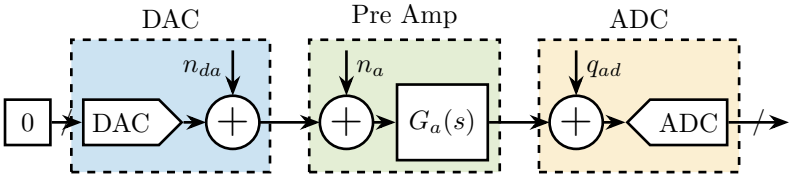
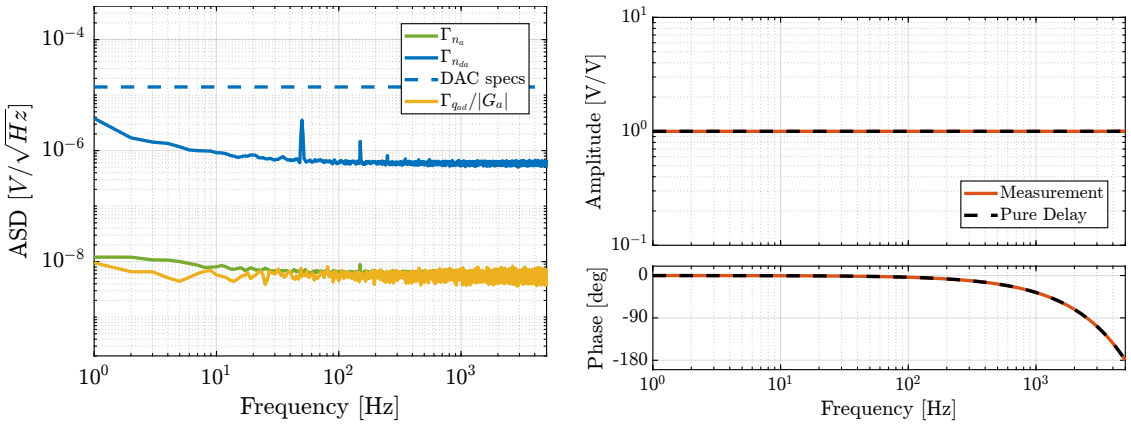


Figure 3.7: Measurement of the DAC output voltage noise. A pre-amplifier with a gain of 1000 is used before measuring the signal with the ADC.

Delay from ADC to DAC To measure the transfer function from DAC to ADC and verify that the bandwidth and latency of both instruments is sufficient, a direct connection was established between the DAC output and the ADC input. A white noise signal was generated by the DAC, and the ADC response was recorded.

The resulting frequency response function from the digital DAC signal to the digital ADC signal is presented in Figure 3.8b. The observed frequency response function corresponds to exactly one sample delay, which aligns with the specifications provided by the manufacturer.



(a) Output noise of the DAC

(b) Transfer function from DAC to ADC

Figure 3.8: Measurement of the output voltage noise of the ADC (a) and measured transfer function from DAC to ADC (b) which corresponds to a "1-sample" delay.

3.4 Piezoelectric Voltage Amplifier

Output Voltage Noise The measurement setup for evaluating the PD200 amplifier noise is illustrated in Figure 3.9. The input of the PD200 amplifier was shunted with a 50 resistor to ensure that only the inherent noise of the amplifier itself was measured. The pre-amplifier gain was increased to produce a signal substantially larger than the noise floor of the ADC. Two piezoelectric stacks from the APA95ML were connected to the PD200 output to provide an appropriate load for the amplifier.

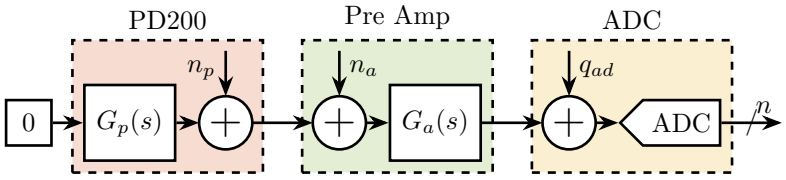


Figure 3.9: Setup used to measured the output voltage noise of the PD200 voltage amplifier. A gain $G_a = 1000$ was used for the instrumentation amplifier.

The Amplitude Spectral Density $\Gamma_n(\omega)$ of the signal measured by the ADC was computed. From this, the Amplitude Spectral Density of the output voltage noise of the PD200 amplifier n_p was derived, accounting for the gain of the pre-amplifier according to (3.1).

$$\Gamma_{n_p}(\omega) = \frac{\Gamma_n(\omega)}{|G_p(j\omega)G_a(j\omega)|} \tag{3.1}$$

The computed Amplitude Spectral Density of the PD200 output noise is presented in Figure 3.10. Verification was performed to confirm that the measured noise was predominantly from the PD200, with negligible contributions from the pre-amplifier noise or quantization noise. The measurements from all six amplifiers are displayed in this figure.

The noise spectrum of the PD200 amplifiers exhibits several sharp peaks. While the exact cause of

these peaks is not fully understood, their amplitudes remain below the specified limits and should not adversely affect system performance.

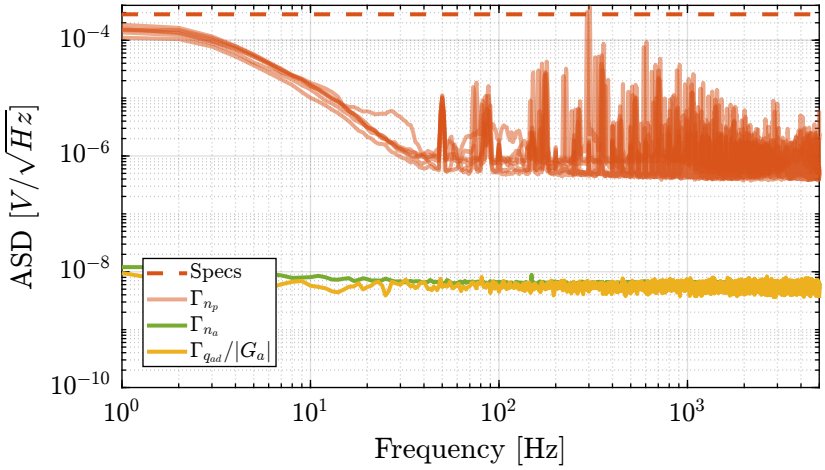


Figure 3.10: Measured output voltage noise of the PD200 amplifiers

Small Signal Bandwidth The small signal dynamics of all six PD200 amplifiers were characterized through frequency response measurements.

A logarithmic sweep sine excitation voltage was generated using the Speedgoat DAC with an amplitude of $0.1\,V$, spanning frequencies from 1 Hz to 5 kHz. The output voltage of the PD200 amplifier was measured via the monitor voltage output of the amplifier, while the input voltage (generated by the DAC) was measured with a separate ADC channel of the Speedgoat system. This measurement approach eliminates the influence of ADC-DAC-related time delays in the results.

All six amplifiers demonstrated consistent transfer function characteristics. The amplitude response remains constant across a wide frequency range, and the phase shift is limited to less than 1 degree up to 500Hz, well within the specified requirements.

The identified dynamics shown in Figure 3.11 can be accurately modeled as either a first-order low-pass filter or as a simple constant gain.

3.5 Linear Encoders

To measure the noise n of the encoder, the head and ruler were rigidly fixed together to ensure that no actual motion would be detected. Under these conditions, any measured signal y_m would correspond solely to the encoder noise.

The measurement setup is shown in Figure 3.12. To minimize environmental disturbances, the entire bench was covered with a plastic bubble sheet during measurements.

The amplitude spectral density of the measured displacement (which represents the measurement noise) is presented in Figure 3.13. The noise profile exhibits characteristics of white noise with an amplitude of approximately 1 nm RMS, which complies with the system requirements.

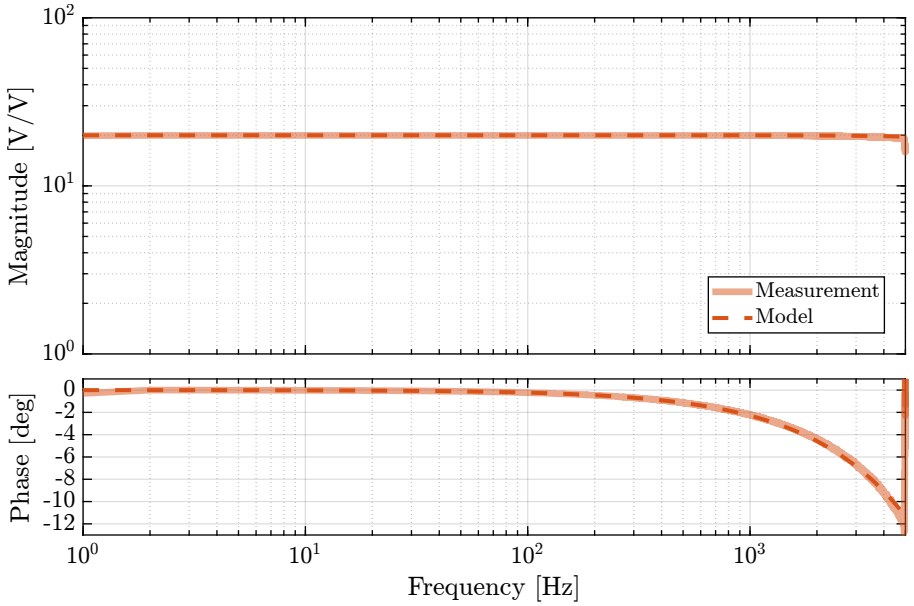


Figure 3.11: Identified dynamics from input voltage to output voltage

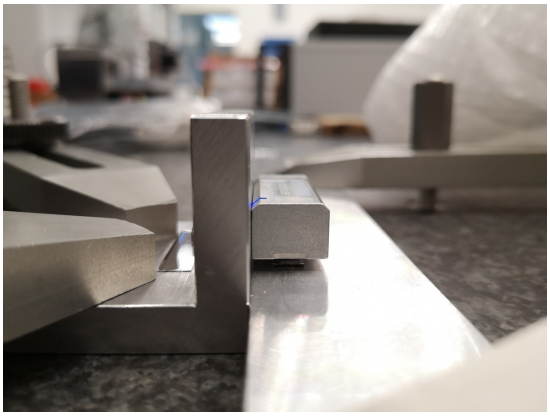


Figure 3.12: Test bench used to measured the encoder noise

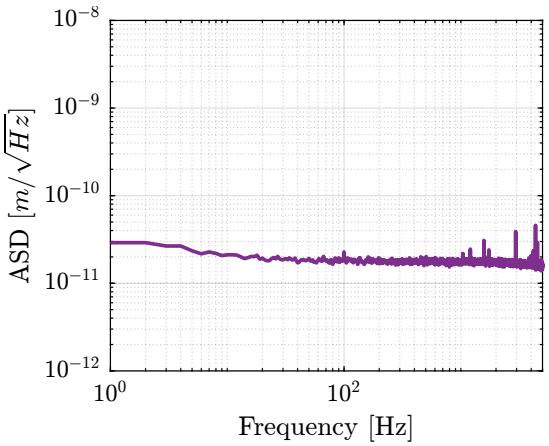


Figure 3.13: Measured Amplitude Spectral Density of the encoder noise

3.6 Noise budgeting from measured instrumentation noise

After characterizing all instrumentation components individually, their combined effect on the sample's vibration was assessed using the multi-body model developed earlier.

The vertical motion induced by the noise sources, specifically the ADC noise, DAC noise, and voltage amplifier noise, is presented in Figure 3.14. The contribution from encoder noise was found to be negligible and is therefore not shown here.

The total motion induced by all noise sources combined is approximately 1.5 nm RMS, which remains

well within the specified limit of 15 nm RMS. This confirms that the selected instrumentation, with its measured noise characteristics, is suitable for the intended application.

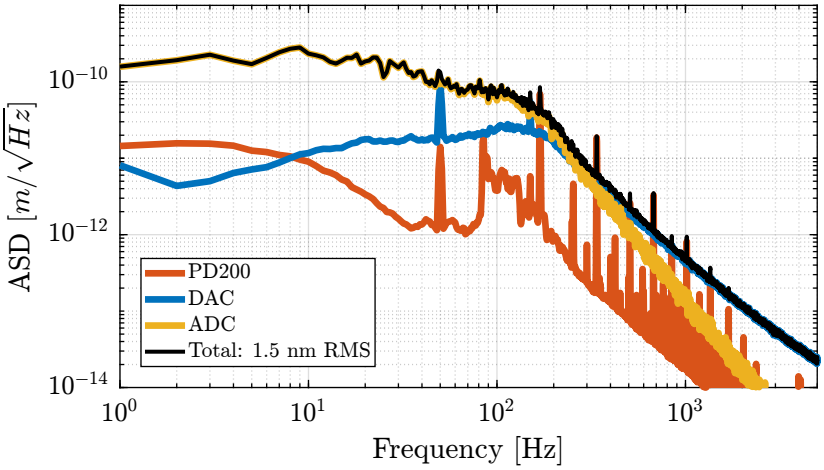


Figure 3.14: Closed-loop noise budgeting using measured noise of instrumentation

Conclusion

This section has presented a comprehensive approach to the selection and characterization of instrumentation for the nano active stabilization system. The multi-body model developed earlier proved invaluable for incorporating instrumentation components and their associated noise sources into the system analysis. From the most stringent requirement (i.e. the specification on vertical sample motion limited to 15 nm RMS), detailed specifications for each noise source were methodically derived through dynamic error budgeting.

Based on these specifications, appropriate instrumentation components were selected for the system. The selection process revealed certain challenges, particularly with voltage amplifiers, where manufacturer datasheets often lacked crucial information needed for accurate noise budgeting, such as amplitude spectral densities under specific load conditions. Despite these challenges, suitable components were identified that theoretically met all requirements.

The selected instrumentation (including the IO131 ADC/DAC from Speedgoat, PD200 piezoelectric voltage amplifiers from PiezoDrive, and Vionic linear encoders from Renishaw) was procured and thoroughly characterized. Initial measurements of the ADC system revealed an issue with force sensor readout related to input bias current, which was successfully addressed by adding a parallel resistor to optimize the measurement circuit.

All components were found to meet or exceed their respective specifications. The ADC demonstrated noise levels of $5.6\,\mu V/\sqrt{\text{Hz}}$ (versus the $11\,\mu V/\sqrt{\text{Hz}}$ specification), the DAC showed $0.6\,\mu V/\sqrt{\text{Hz}}$ (versus $14\,\mu V/\sqrt{\text{Hz}}$ required), the voltage amplifiers exhibited noise well below the $280\,\mu V/\sqrt{\text{Hz}}$ limit, and the encoders achieved 1 nm RMS noise (versus the 6 nm RMS specification).

Finally, the measured noise characteristics of all instrumentation components were incorporated into the multi-body model to predict the actual system performance. The combined effect of all noise sources was estimated to induce vertical sample vibrations of only 1.5 nm RMS, which is substantially below the 15 nm RMS requirement. This rigorous methodology spanning requirement formulation, component selection, and experimental characterization validates the instrumentation's ability to fulfill the nano active stabilization system's demanding performance specifications.

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